A

Seminar report

On

FERROELECTRIC RAM [FRAM]

Submitted in partial fulfillment of the requirement for the award of degree of Bachelor of Technology in Computer Science

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Acknowledgement

I would like to thank respected Mr…….. and Mr. ……..for giving me such a wonderful opportunity to expand my knowledge for my own branch and giving me guidelines to present a seminar report. It helped me a lot to realize of what we study for.

Secondly, I would like to thank my parents who patiently helped me as i went through my work and helped to modify and eliminate some of the irrelevant or un-necessary stuffs.

Thirdly, I would like to thank my friends who helped me to make my work more organized and well-stacked till the end.

Next, I would thank Microsoft for developing such a wonderful tool like MS Word. It helped my work a lot to remain error-free.

Last but clearly not the least, I would thank The Almighty for giving me strength to complete my report on time.

Preface

I have made this report file on the topic **FERROELECTRIC RAM [FRAM]**; I have tried my best to elucidate all the relevant detail to the topic to be included in the report. While in the beginning I have tried to give a general view about this topic.

My efforts and wholehearted co-corporation of each and everyone has ended on a successful note. I express my sincere gratitude to ……..who assisting me throughout the preparation of this topic. I thank him for providing me the reinforcement, confidence and most importantly the track for the topic whenever I needed it.

ABSTRACT

Ferroelectric memory is a new type of semiconductor memory, which exhibit short programming time, low power consumption and nonvolatile memory, making highly suitable for application like contact less smart card, digital cameras which demands many memory write operations.

A ferroelectric memory technology consists of a complementary metal-oxide-semiconductor (CMOS) technology with added layers on top for ferroelectric capacitors. A ferroelectric memory cell has at least one ferroelectric capacitor to store the binary data, and one transistor that provide access to the capacitor or amplify its content for a read operation. Once a cell is accessed for a read operation, its data are presented in the form of an analog signal to a sense amplifier, where they are compared against a reference voltage to determine their logic level.

Ferroelectric memories have borrowed many circuit techniques (such as folded-bitline architecture) from DRAM's due to similarities of their cells and DRAM's maturity. Some architectures are reviewed here.

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INTRODUCTION

Before the 1950's, ferromagnetic cores were the only type of random-access, nonvolatile memories available. A core memory is a regular array of tiny magnetic cores that can be magnetized in one of two opposite directions, making it possible to store binary data in the form of a magnetic field. The success of the core memory was due to a simple architecture that resulted in a relatively dense array of cells. This approach was emulated in the semiconductor memories of today (DRAM's, EEPROM's, and FRAM's). Ferromagnetic cores, however, were too bulky and expensive compared to the smaller, low-power semiconductor memories. In place of ferromagnetic cores ferroelectric memories are a good substitute. The term "ferroelectric' indicates the similarity, despite the lack of iron in the materials themselves.

Ferroelectric memory exhibit short programming time, low power consumption and nonvolatile memory, making highly suitable for application like contact less smart card, digital cameras which demanding many memory write operations. In other word FRAM has the feature of both RAM and ROM. A ferroelectric memory technology consists of a complementry metal-oxide-semiconductor (CMOS) technology with added layers on top for ferroelectric capacitors. A ferroelectric memory cell has at least one ferroelectric capacitor to store the binary data, and one or two transistors that provide access to the capacitor or amplify its content for a read operation.

A ferroelectric capacitor is different from a regular capacitor in that it substitutes the dielectric with a ferroelectric material (lead zirconate titanate (PZT) is a common material used)-when an electric field is applied and the charges displace from their original position spontaneous polarization occurs and displacement becomes evident in the crystal structure of the material. Importantly, the displacement does not disappear in the absence of the electric field. Moreover, the direction of polarization can be reversed or reoriented by applying an appropriate electric field.

A hysteresis loop for a ferroelectric capacitor displays the total charge on the capacitor as a function of the applied voltage. It behaves similarly to that of a magnetic core, but for the sharp transitions around its coercive points, which implies that even a moderate voltage can disturb the state of the capacitor. One remedy for this would be to modify a ferroelectric memory cell including a transistor in series with the ferroelectric capacitor. Called an access transistor, it wo control the access to the capacitor and eliminate the need for a square like hysteresis loop compensating for the softness of the hysteresis loop characteristics and blocking unwanted disturb signals from neighboring memory cells.

Once a cell is accessed for a read operation, its data are presented in the form of an anal signal to a sense amplifier, where they are compared against a reference voltage to determine the logic level.

Ferroelectric memories have borrowed many circuit techniques (such as folded-bitline architecture) from DRAM's due to similarities of their cells and DRAM's maturity. Some architectures reviewed are,

- Wordline-parallel Plateline (WL//PL);

- Bitline-parallel Plateline (BL//PL);
- Segmented plateline (segmented PQ);
- Merged Wordline/Plateline architecture (ML);

BASIC MEMORY CELL STRUCTURE

A ferroelectric memory cell, known as IT- IC (one transistor, one capacitor) ,structure which is similar to that of DRAM. The difference is that ferroelectric film is used as its storage capacitor rather than paraelectric material as in DRAM.

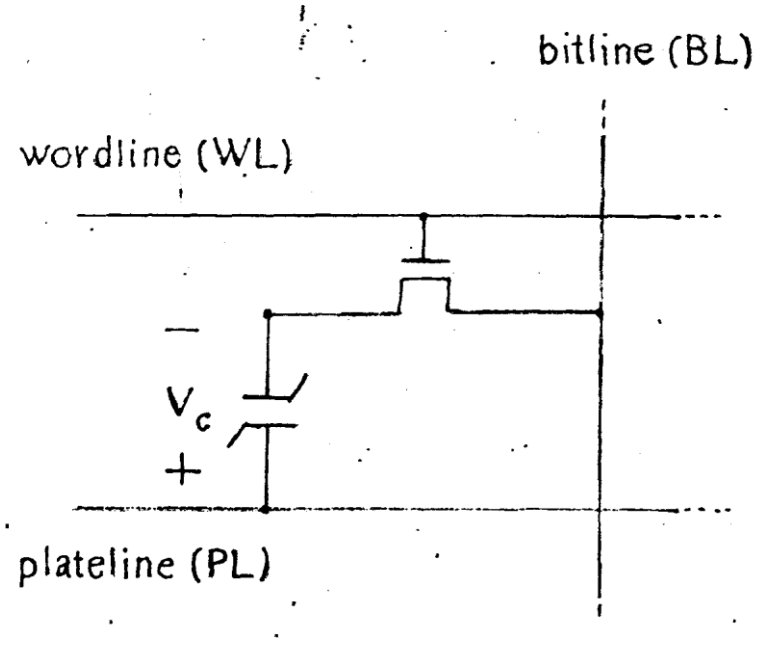


Fig. 1. Ferroelectric IT-IC structure

Figure above shows memory cell structure, consists of a single ferroelectric capacitor that is connected to a Plateline(PL) at one end and, via an access transistor, to a Bitline(BL) at the other end. Raising the wordline (WL) and hence turning ON the access transistor accesses the cell.

As shown in fig 2 ferroelectric memory technology consists of a CMOS technology with added layers on top for ferroelectric capacitors. Therefore, by masking parts of the design that are not using ferroelectric capacitors, CMOS digital and analog circuits can be integrated together with ferroelectric memories, all in the same chip. Ferroelectric capacitors to sit directly on the top of the transistors by means of stacked vias, hence reducing cell area.

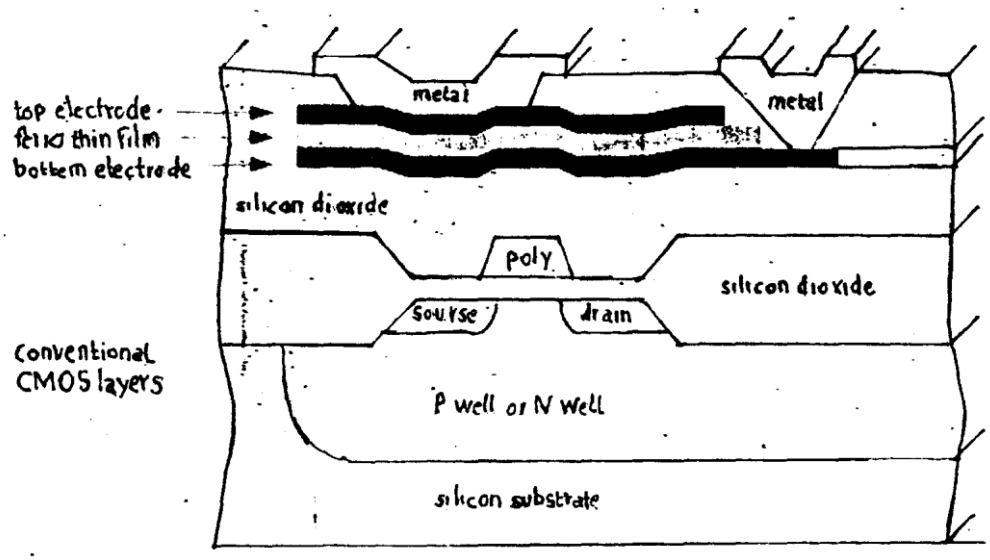


Fig. 2. Ferroelectric Capacitor layers on top of conventional CMOS process

FERROELECTRIC CAPACITOR

The basic building block of FRAM is the Ferroelectric capacitor. A ferroelectric capacitor physically distinguished from a regular capacitor by substituting the dielectric with a ferroelectric material. In a regular dielectric, upon the application of an electric field, positive and negative charges will be displaced from their original positions-a concept that is characterized polarization. This polarization, or displacement, will vanish, however, when the electric field return back to zero. In, a ferroelectric material, on the other hand, there is a spontaneous polarization displacement that is inherent to the crystal structure of the material and does not disappear in the absence of electric field. The direction of this polarization can be reversed or reoriented by applying an appropriate electric field.

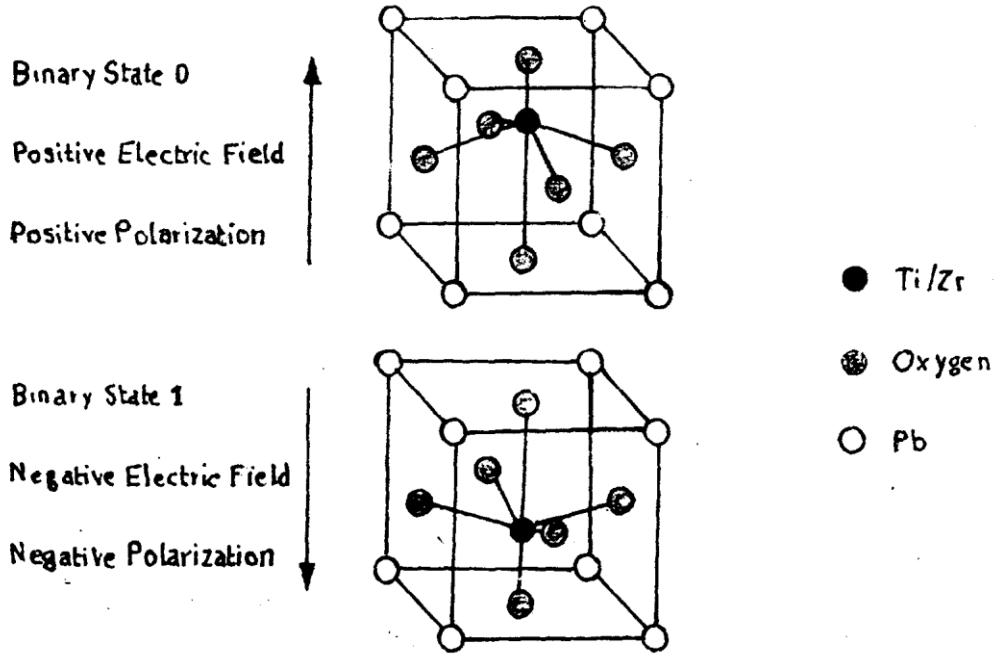


Fig. 3. Two stable state in a Ferroelectric Material

Widely used dielectric material is Lead Zirconate Titanate (PZT) with formula $Pb(Zr_x\ Ti_{1-x})03$. Fig 3 illustrates a unit cell of this material. The central atom in this unit cell either Titanium (Ti) or Zirconium (Zi), depending on the contribution of each atom to the material formula. Lead (Pb) are at the corner of the cube and Oxygen (02) at the face center of the cub lattices.

When the electric field applied to ferroelectric crystal, the central atom moves in the direction of the field. As the atom moves with in the crystal, it passes through an energy barrier causing a charge spike. Although the polarization of each individual unit cell is tiny, the non polarization of several domains-each consisting of a number of aligned unit cells-can be large enough for detection using standard sense amplifier designs. The gross effect of polarization is nonzero charge per unit area of the ferroelectric capacitor that exists at 0 V and does not disappear over time. Which exhibit a hysterisis loop like ferromagnetic material and nonvolatile property.

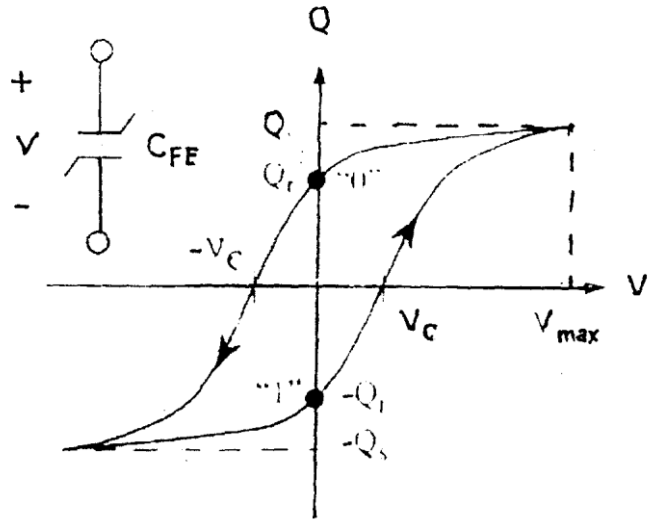


Fig. 4 Hysteresis loop characteristic of a Ferroelectric Capacitor

A hysteresis loop for a ferroelectric capacitor, as shown in Fig. 4, displays the total charge on the capacitor as a function of the applied voltage. When the voltage across the capacitor is 0 V, the capacitor assumes one of the two stable states: "0" or "1". The total charge stored on the capacitor is Q_r. for a "0" or for a "1". A "0" can be switched to a "1" by applying a negative voltage pulse across the capacitor. By doing so, the total charge on the capacitor is reduced by $2Q_r$, a change of charge that can be sensed by the sense circuitry. Similarly, a "1" can be switched back to a "0" by applying a positive voltage pulse across the capacitor, hence restoring the capacitor charge to $+Q_r$. These characteristics are all very similar to those of a magnetic core except the hysteresis loop of a ferroelectric capacitor does not have sharp transitions around its coercive points:-Vc, and +Vc. This reflects a partial switching of electric domains in a ferroelectric capacitor, and further implies the even a voltage half of V_{max} , can disturb the state of the capacitor. As a result, it is impossible access a ferroelectric capacitor in a cross-point array without disturbing the capacitors on the same row or column.

As a remedy this situation would be to modify the ferroelectric material processing in order to create a square-like hysteresis loop. As magnetic core form a core memory. This is a technical development that we may expect in near future.

Another approach is to modify a ferroelectric memory cell by including a transistor in series with the ferroelectric capacitor. The transistor, called the access transistor, controls the access to the capacitor and eliminates the need for square-like hysteresis loop. When the access transistor is "OFF", the FE capacitor remains disconnected from bitline (BL) and hence cannot be

disturbed. When the access transistor is "ON", the FE capacitor is connected to the bitline and can be written to or read by the plateline (PL). In other words, the presence of an access transistor in series with the ferroelectric capacitor compensates for the softness of its hysteresis loop characteristics and block unwanted disturb signals from neighbouring memory cells.

BASIC MEMORY CELL OPERATION

The principles of operation of ferroelectric capacitor and ferromagnetic core are similar. We first discuss the principle of operation of ferromagnetic memories, which make it easier to understand the operation of ferro electric cell.

FERROMAGNETIC CORE

A core memory, as shown in Fig. 5, consists of a regular array of tiny .magnetic cores that can be magnetized in one of two opposite directions, hence storing binary data in the form of a magnetic field. A write access into a core consists of sending simultaneous current pulses through the core via its x-access and y-access wires. Depending on the directions of the current pulses, a core is magnetized in a "0" or a "1" direction. The basic assumption here is that only the core that receives two simultaneous current pulses is affected. All the remaining cores, including those that receive one current pulse or none, retain their original magnetization.

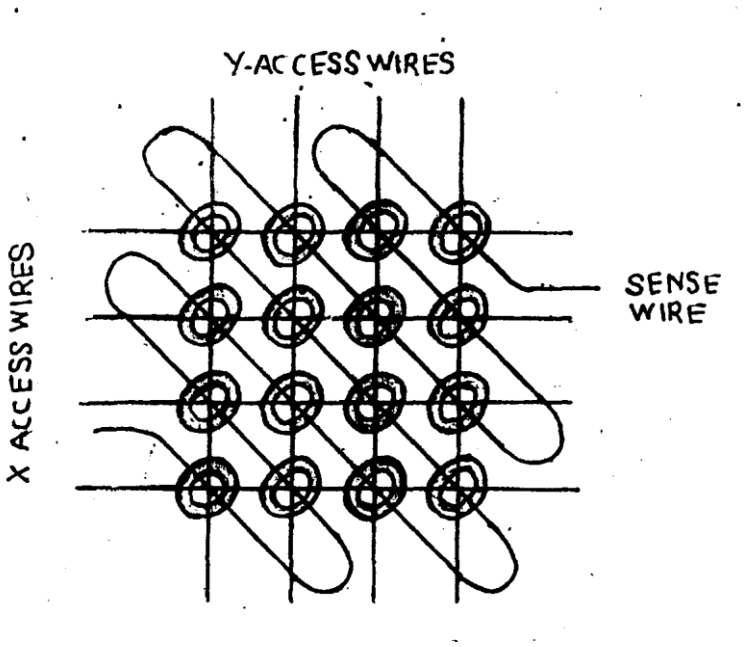


Fig. 5. Two-dimension array of Ferroelectric

A read access Consists of a write access followed by sensing. We write a "0" to the core is order to discover the original data content of the core. If the original content of the core is a "1", writing a "0" would mean changing the magnetic direction of the core. This induces a large current spike on the sense wire. On the other hand, there will be no current spike on the sensing wire if the original content of the core was also a "0." Therefore, by sensing the presence of a current spike or the sensing wire, the original data of the accessed core are determined.

The read operation as explained above is destructive since a "0" is written to any core that is accessed for a read. The original data, however, are saved at the sense amplifier and can be restored back into the accessed core. In other words, a read access is only complete after the second write that restores the original data.

FRAM WRITE OPERATION

The cell consists of a single ferroelectric capacitor that is connected to a PL at one end and via an access transistor, to a BL at the other end. The cell is accessed by raising the wordline (WL) and hence turning ON the access transistor. The access is one of two types: a write access or a read access.

The timing diagram for a write operation is shown in Fig.6. To write a "1" into the memory cell, the BL is raised to V_{DD}. Then the WL is raised to $V_{DD} + V_r$ (known as boosted V_{DD}) where V_T is the threshold voltage of the access transistor. This allows a full V_{DD} to appear across the ferroelectric capacitor ($-V_{DD}$) according to the voltage convention adopted in Figure). At this time, the state of the ferroelectric capacitor is independent of the initial state of the FE capacitor, as shown in Figure. At this time the state of ferroelectric is independent of its initial state. Next, the PL is pulsed, that is, pulled UP to V_{DD} and subsequently pulled back down to ground. Note that the WL stays activated until the PL is

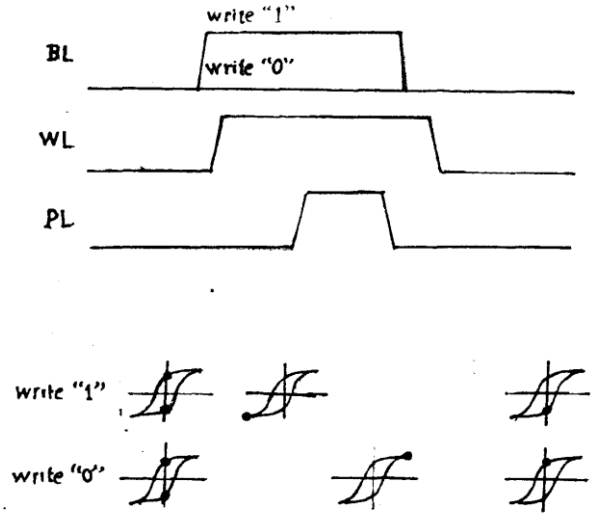


Fig. 6. Timing diagram for a write operation of the Memory Cell

pulled down completely and the BL is driven back to zero. The final state of the capacitor is a negative charge state S_1. Finally, deactivating the WL leaves this stare undisturbed until the next access.

To write a "0" into the cell, the BL is driven to 0V prior to activating the WL. The rest of the operation is similar to that of writing a "1" as shown in Fig. 6.

The written data is held in the cell even though the selection of the wordline is changed to non selected state (i.e. transistor is OFF), so it is nonvolatile. The level of polarization that correspond to the data remain as the state of remnant polarization after the applied voltage is removed.

FRAM READ OPERATION

Similar to ferromagnetic capacitor, read operation is destructive. The original data, however, are saved at sense amplifier and can be restored back. In another word a read access is. Only complete after the second write that restores the original data. -.

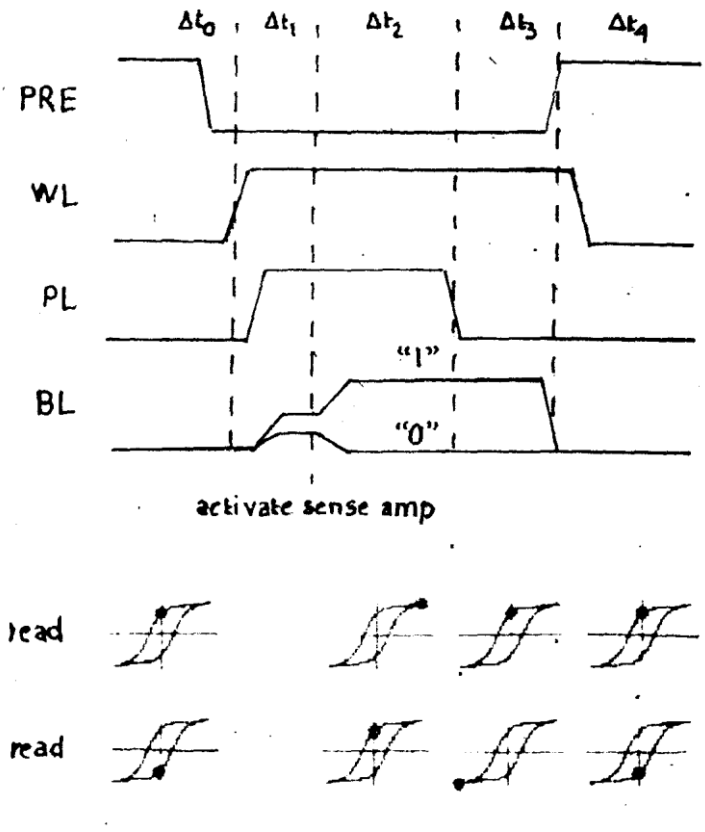


Fig. 7. Timing diagram of Read Operation of the Memory Cell

The timing diagram for a read access is shown in Fig. 7. A read access begins by precharging the BL to 0V, followed by activating the WL (∆to). This establishes a capacitor divider consisting of C_{FE} and C_{BL} between the PL and the ground. Where C_{BL} represent the total amount of parasitic capacitance of the bit line. Depending on the data stored, the capacitance of the FE capacitor can be: approximated by C_o or C_1. That is C_{BL} and C_0 or C_1 act as a voltage divider, therefore the voltage developed on the bitline (Vx) can be one of the two. .

$$V_X = \begin{cases} V_0 = \dfrac{C_0}{C_0 + C_{BL}} V_{DD} & \text{If the stored data is a “0”} \\ V_1 = \dfrac{C_1}{C_1 + C_{BL}} V_{DD} & \text{If the stored data is a’} \end{cases}$$

At this point, the sense amplifier is activated to drive the BL t V_{DD} if the voltage developed on the BL is V_1 or to 0V if the voltage on the BL is V_o. The WL is kept activated until the sensed voltage on the BL restores the original data back into the memory cell and the BL is precharged back to 0V. The sense amplifier can discriminate between a “0” and “1” voltage signal on the BL. This is only possible if a reference voltage, midway between a “0’ and a “1” signal.

SENSING SCHEMES

The read access as presented above is known as the step-sensing approach, since a step voltage (the rising edge of a pulse) is applied to the PL prior to sensing. An alternative is the pulse-sensing approach in which a full pulse is applied to the PL prior to activating the sense amplifiers (refer to Fig.8). The charge transferred to the BL in a pulse sensing scheme is either zero for a stored "0" or $2Q_T$ for a stored "I". Equivalently the voltage developed on the BL is either 0V for a stored "0" or V_1 -V_o for a stored "1".

In both step- and pulse-sensing schemes, the voltage difference on the BL that is developed by a stored "1" and a stored "0" is equal to V_1 — V_0. The common-mode voltage, however, is equal to $(V_1 + V_o)/2$ in the step-sensing approach, as compared to $(V_1 - V_o)/2$ in the pulse-sensing approach. Therefore, the step-sensing approach provides a higher common-mode voltage on the BL that simplifies the sense amplifier design when a bias voltage is required. Another advantage of the step-sensing approach is that it provides a faster read access, as the sensing does not wait for the PL to be pulled low.

Both step- and pulse-sensing approaches restore "1", but only the step-sensing approach fully reinforces a "0". To substantiate this point, note that during a read operation in a step-sensing approach, an FE capacitor storing a "0" experiences a voltage sequence Of 0V, V_{DD} — V_0 – V_{DD} and 0V (a full-V_{DD} excursion). In a pulse-sensing approach, the corresponding voltage sequence is 0V, V_{DD} - V_o, and 0 V (aV_{DD} - V_o excursion). None of the two voltage sequences upsets the

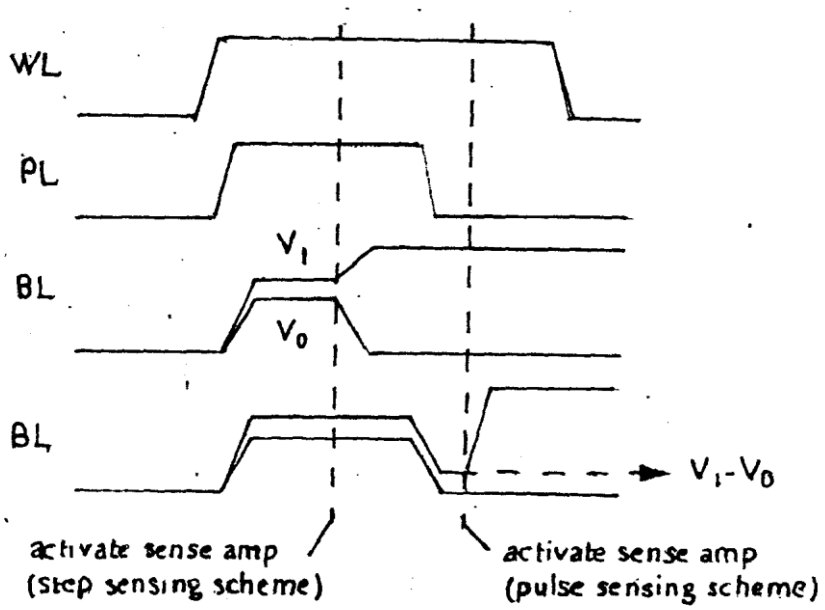


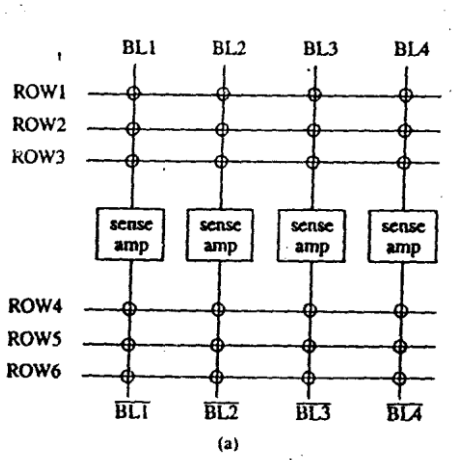
Fig. 8. Timing' Diagram for Read operation based on step-sensing scheme and pulse sensing scheme

original data (i.e. "0") of the FE capacitor. However, the latter provides a weak reinforcement of "0" by applying a voltage less than V_{DD} across the capacitor. This seems to deteriorate the capacitor's long-term retention performance. To remedy this situation, a second pulse must be applied to the PL to fully restore the "0" into the capacitor. This implies that the cycle time for the pulse-sensing approach can be twice as large as that of the step-sensing approach.

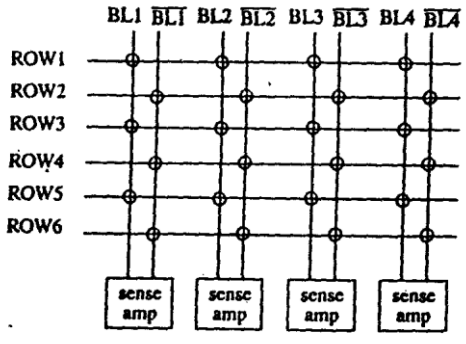
The pulse-sensing approach applies both the leading edge and the trailing edge of the voltage pulse to the FE capacitor prior to sensing. The trailing edge eliminates the non switching part of polarization that was introduced on the BL by the rising edge and therefore bypasses the effect of non switching part of polarization and its process variations altogether. This seems to be the only advantage of the pulse sensing approach over the step-sensing approach.

FERROELECTRIC MEMORY ARCHITECTURE

Ferroelectric memories have borrowed many circuit techniques from DRAM's due to similarities of their cells and DRAM's mature architecture. A folded-bitline architecture, for example, that was first introduced to replace an older open-bitline architecture in DRAM is now well adopted in FRAM. The bitlines are folded to lie on the same side of a sense amplifier, as shown in Fig. 9, instead of lying open on opposite sides of the sense amplifier, to reduce chances of any bitline mismatch that



(a)



(b)

Fig. 9. Block diagram of ferroelectric Memory with

(a) an open bitline architecture and
(b) a fold bitline architecture

could occur due to process variations. On the other hand, the requirement for pulsing the plateline in an FRAM has called for original circuit techniques that were not required in a DRAM. There are various memory architectures that have been developed for an FRAM with moving plateline. We discuss these architectures in Section A to D.

A. WORDLINE-PARALLEL PLATELINE (WL//PL)

Fig. 10. shows a simplified block diagram of a WL/ /PL architecture. As its name suggests, the PL is run parallel to the WL in this architecture. When a WL and PL pair is activated, an entire row that shares the same WL and PL is accessed at once. It is impossible, in this architecture, to access a single cell without accessing an entire row. This is in fact common in almost every RAM since the adjacent cells in a row store the adjacent bits of a byte, which are accessed simultaneously. Sometimes, the PL in this architecture is shared between two adjacent rows to reduce the array area by eliminating a metal line. In this case, the unaccessed cells connected to an activated PL can be disturbed. This is due to the voltage that develops across the FE capacitors of the non selected cells with the active PL. Ideally. This voltage to be zero because the storage nodes of the cells should be floating. However, the parasitic capacitance of a storage node forms a capacitor divider with the FE capacitor itself and produces a nonzero voltage across the FE capacitor. For a stored ‘0’. data, the disturb voltage is in the direction that reinforces the “0”.

For a stored "1" data, however, the disturb voltage is in the direction of flipping the data. If this voltage is small enough (much less than the coercive voltage of the FE capacitor), it can be ignored. Otherwise, a data "1" can be flipped by a sequence of small voltage disturbances.

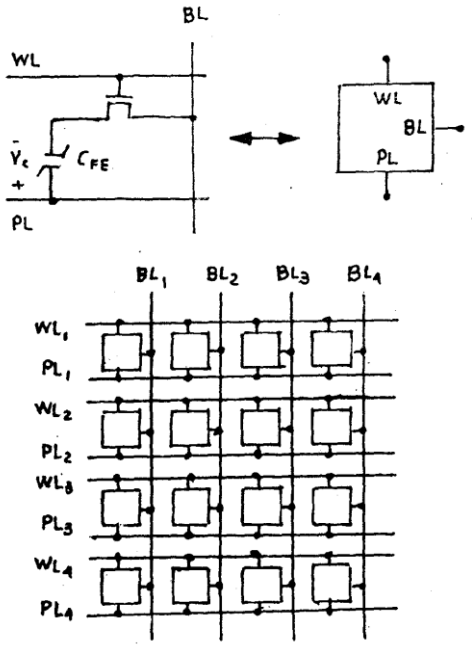


Fig. 10. Block Diagram of Ferroelectric Memory with WL//PL architecture

B. BITLINE-PARALLEL PLATELINE (BL//PL)

Fig. 11. shows an array architecture in which the PL is run parallel to the BL, hence the name BL//PL for the architecture. Unlike the previous architecture, only a single memory cell can be selected by a simultaneous activation of a WL and a PL. This is the memory cell that is located at the Intersection of the WL and the PL. It is possible to select more than one memory cell in a row by activating their corresponding platelines.

This architecture absorbs the function of a y-decoder in the selection of the platelines. File activation of the sense an is controlled by the same signal

as the PL. Therefore, only one sense amplifier is activated if only one memory cell needs to be accessed. This reduces the power consumption significantly.

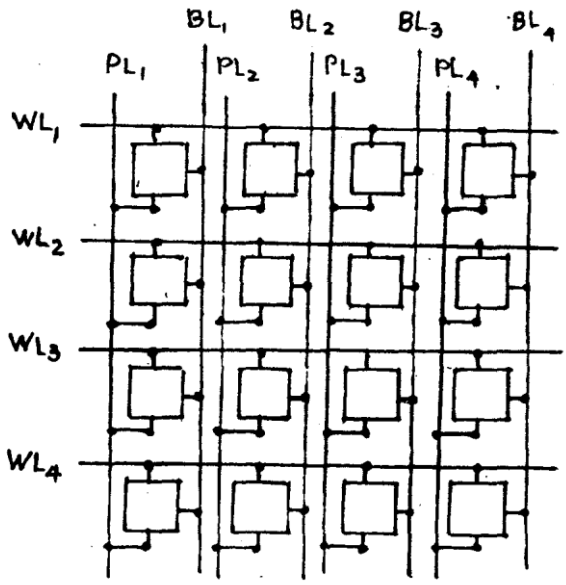


Fig.11. Block Diagram of Ferroelectric Memory with BL//PL architecture

On the other hand, if an entire row needs to be accessed, then all the platelines are selected simultaneously, hence increasing the dynamic power consumption due to charging and discharging the platelines.

The main disadvantage of this architecture is that activating a PL could disturb all the cells in the corresponding column. This is very similar to the situation discussed for the WL//PL architecture with PL shared between two adjacent rows.

C. SEGMENTED PLATELINE (SEGMENTED PL)

WL//PL architecture is power consuming and relatively slow because the PL is activated in its full length to access all the cells in the row at once.

Also, a BL//PL architecture could be power consuming if multiple platelines are activated to access multiple memory cells in the selected row.

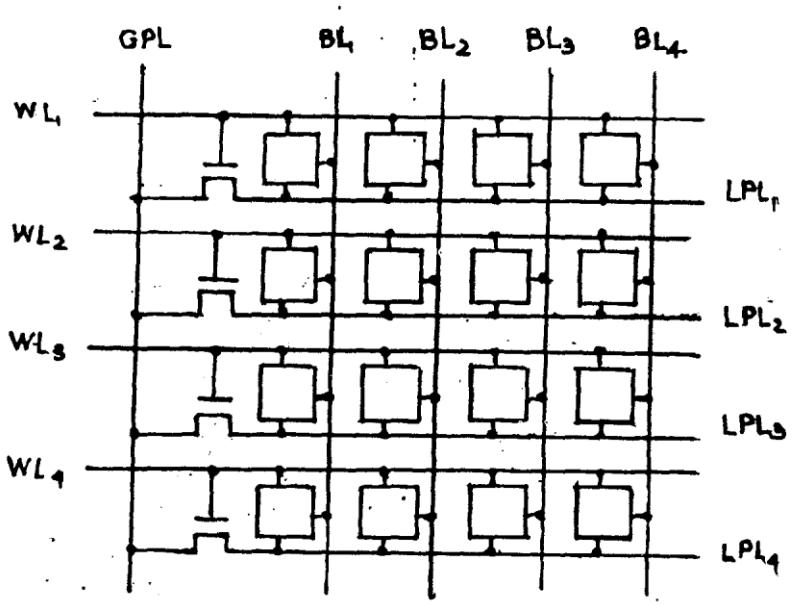


Fig. 12. Block Diag, of Ferroelectric Memory with Segmented-PL archilecture

For larger arrays, the PL can be segmented into local platelines (LPL's) that run parallel to the WL and controlled by a global plateline (GPL) that runs parallel to the BL. As shown in Fig. 12. a GPL is ANDed with the WL to generate the signal for the LPL. Since the LPL is only connected to a few memory cells (eight in this example), it can respond much faster than a PL in the WL//PL architecture Also, since the WL gates the GPL, there is no disturbance to the non selected cells in the column, as it was in the BL//PL architecture.

Among the three architectures discussed so far, the segmented-PL architecture seems to be the most feasible architecture for a large-density ferroelectric memory. A compromise between speed and power consumption can be made by choosing the number of LPL's per GPL.

D. MERGED WORDLINE//PLATELINE (ML) ARCHITECTURE

A WL and its neighboring PL in WL//PL architecture can be merged to form a single merged line (ML) in this architecture. Fig. 13. shows the circuit diagram of two IT-IC memory cells or a single 2T-2C cell connected to two ML's (ML1 and ML2) and two bitlines (BLn and BLn+l).

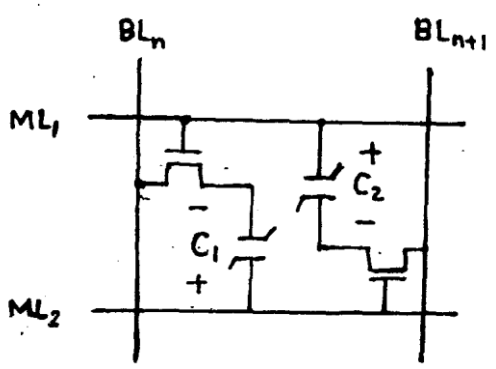


Fig. 13. Circuit Diagram of a pair of Ferroelectric Memory Cells for a Merged-line architecture

Compared to a WL//PL architecture, the ML architecture enjoys a shorter read access time, as the PL capacitance is-now divided equally between two merged lines. This allows the merged line to respond twice as fast, assuming that the original wordline capacitance is negligible compared to the original plateline capacitance. The read/write cycle time, however, remains the same in both architectures. This is due to the fact that four transitions are required for a full read/write operation, instead of two in WL//PL architecture. Finally, the ML architecture can achieve higher density compared to the WL//IPL architecture due to reduced number of access wires, that is, using a single merged line instead of a wordline and a plateline. This higher density

comes at the expense of complicated processing steps such as stacking the bottom electrode of the FE capacitor right on top of the transistor gate and providing a side contact (plug) to the top electrode from the transistor source/drain area.

COMPARISON

The memory cell of FRAM is configured with one transistor and one capacitor is DRAM. It can also hold data even when the power is switched off as can flash memory, which is a representative nonvolatile memory device. FRAM has a well-balanced combination of features of both RAM and ROM.

FRAM can be rewritten more than 10^8 times, which is comparable to DRAM or SRAM in actual applications, while flash memory can be written to 10^5 times at maximum.

FRAM dose not need an erase operation before it is rewritten. This is similar to DRAM or SRAM. On the other hand, Flash memory (or specific sectors) must he erased once to he rewritten. FRAM is characteristically easy to operate because it does not need to he refreshed to hold data unlike DRAM.

	FRAM	EEPROM	Flash Memory	DRAM	SRAM
Memory Type	Non-volatile	Non-volatile	Non-volatile	Volatile	Volatile
Read Cycle	100ns	200ns	120ns	70ns	85ns
Write Cycle	100ns	10us	100us	70ns	85ns
Power Consumption	1nJ	1uJ	2uJ	4uJ	3uJ
Current to retain Data	Unnecessary	Unnecessary	Unnecessary	Necessary	Necessary
Internal Write Voltage	2V-5V	14V	9V	3.3V	3.3V
Cell Structure	1T-1C	2T	1T	1T-1C	6T,4T+R
Area/Cell	4	3	1	2	4

CONCLUSION

Looking toward the future, we-anticipate progress in three areas: density, access and cycle times, and use as an embedded memory in system-on-chip technology. The density of commercial ferroelectric memory has improved dramatically over the past three years from 64 to 256 kb, with I-Mb densities expected soon.

Ferroelectric memories, on the other hand, are superior to EPROM's and Flash memories in terms of write-access time and overall power consumption, and hence, target applications where a nonvolatile memory is required with such features. Two examples of such applications are Contactless smart cards and digital cameras. Contactless smart cards require nonvolatile memories with low power consumption, as they use only electromagnetic coupling to power up the electronic chips on the card. Digital cameras require

both low power consumption and fast frequent writes in order to store and restore an entire image into the memory in less than 0.1s.

Another advantage of ferroelectric memories over EEPROM's and Flash memories is that they can be easily embedded as part of a larger integrated circuit to provide system-on-a-chip solutions to various applications. Future personal wireless connectivity applications that are battery driven, such as third-generation cellular phones and personal digital assistants, will demand large amounts (multiple megabytes) of nonvolatile storage to retain accessed Internet Web pages, containing compressed video; voice, and data. The density and energy efficiency of writing data to memory would seem to indicate that ferroelectric memory will play a major role in these types of consumer products.

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