

A

Seminar report

On

Bicmos Technology

Submitted in partial fulfillment of the requirement for the award of degree
of Bachelor of Technology in Mechanical

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Preface

I have made this report file on the topic **Bicmos Technology**; I have tried my best to elucidate all the relevant detail to the topic to be included in the report. While in the beginning I have tried to give a general view about this topic.

My efforts and wholehearted co-corporation of each and everyone has ended on a successful note. I express my sincere gratitude towho assisting me throughout the preparation of this topic. I thank him for providing me the reinforcement, confidence and most importantly the track for the topic whenever I needed it.

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CONTENTS

1. INTRODUCTION
2. SYSTEM ON CHIP FUNDAMENTALS
3. ACTIVE DEVICE OPTION FOR ANALOG AND RF SOC DESIGN
 - 3.1.1 BIPOLAR
 - 3.1.2 CMOS
 - 3.1.3 BiCMOS
4. BiCMOS PROCESS TECHNOLOGY FOR RF DIGITAL AND ANALOG CIRCUITS
 - 4.1 TECHNOLOGY DESCRIPTION OF THE STANDARD SUBMICRON PROCESS
 - 4.1.1 DIGITAL CMOS CORE PROCESS
 - 4.1.2 DENSE SRAM
 - 4.1.3 PROCESS INTEGRATION OF THE SiGe DEVICE
5. PASSIVE COMPONENT FOR FULLY INTEGRATED ANALOG AND RF CIRCUITS
 - 5.1 RESISTORS
 - 5.2 CAPACITORS
 - 5.3 INDUCTORS
 - 5.4 VARACTORS

6. BiCMOS TECHNOLOGY PRESENT AND FUTURE
7. CONCLUSION
8. REFERENCES

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1. INTRODUCTION

The history of semiconductor devices starts in 1930's when Lienfed and Heil first proposed the mosfet. However it took 30 years before this idea was applied to functioning devices to be used in practical applications, and up to the late 1980 this trend took a turn when MOS technology caught up and there was a cross over between bipolar and MOS share. CMOS was finding more wide spread use due to its low power dissipation, high packing density and simple design, such that by 1990 CMOS covered more than 90% of total MOS scale.

In 1983 bipolar compatible process based on CMOS technology was developed and BiCMOS technology with both the MOS and bipolar device fabricated on the same chip was developed and studied. The objective of the BiCMOS is to combine bipolar and CMOS so as to exploit the advantages of both at the circuit and system levels. Since 1985, the state-of-the-art bipolar CMOS structures have been converging. Today BiCMOS has become one of the dominant technologies used for high speed, low power and highly functional VLSI circuits especially when the BiCMOS process has been enhanced and integrated in to the CMOS process without any additional steps. Because the process step required for both CMOS and bipolar are similar, these steps can be shared for both of them.

2. SYSTEM ON CHIP (SOC) FUNDAMENTALS

The concept of system-on-chip (SOC) has evolved as the number of gates available to a designer has increased and as CMOS technology has migrated from a minimum feature size of several microns to close to 0.1 μm . Over the last decade, the integration of analog circuit blocks is an increasingly common feature of SOC development, motivated by the desire to shrink the number of chips and passives on a PC board. This, in turn, reduces system size and cost and improves reliability by requiring fewer components to be mounted on a PC board. Power dissipation of the system also improves with the elimination of the chip input-output (I/O) interconnect blocks. Superior matching and control of integrated components also allows for new circuit architectures to be used that cannot be attempted in multi-chip architectures. Driving PC board traces consume significant power, both in overcoming the larger capacitances on the PC board and through larger signal swings to overcome signal cross talk and noise on the PC board. Large-scale microcomputer systems with integrated peripherals, the complete digital processor of cellular phone, and the switching system for a wire-line data-communication system are some of the many applications of digital SOC systems.

Examples of analog or mixed-signal SOC devices include analog modems; broadband wired digital communication chips, such as DSL and cable modems; Wireless telephone chips that combine voice band codes with base band modulation and demodulation function; and ICs that function as the complete read channel for disc drives. The analog section of these chips includes wideband

amplifiers, filters, phase locked loops, analog-to-digital converters, digital-to-analog converters, operational amplifiers, current references, and voltage references. Many of these systems take advantage of the digital processors in an SOC chip to auto-calibrate the analog section of the chip, including canceling de offsets and reducing linearity errors within data converters. Digital processors also allow tuning of analog blocks, such as centering filter-cutoff frequencies. Built-in self-test functions of the analog block are also possible through the use of on-chip digital processors.

Analog or mixed-signal SOC integration is inappropriate for designs that will allow low production volume and low margins. In this case, the nonrecurring engineering costs of designing the SOC chip and its mask set will far exceed the design cost for a system with standard programmable digital parts, standard analog and RF functional blocks, and discrete components. Noise issues from digital electronics can also limit the practicality of forming an SOC with high-precision analog or RF circuits. A system that requires power-supply voltages greater than 3.6 V in its analog or RF stages is also an unattractive candidate for an SOC because additional process modifications would be required for the silicon devices to work above the standard printed circuit board interface voltage of 3.3 V \pm 10%.

Before a high-performance analog system can be integrated on a digital chip, the analog circuit blocks must have available critical passive components, such as resistors and capacitors. Digital blocks, in contrast, require only n-channel metal-oxide semiconductor (NMOS) and p-channel metal-oxide semiconductor (PMOS) transistors. Added process steps may be required to achieve characteristics for resistors and capacitors suitable for high-performance analog

circuits. These steps create linear capacitors with low levels of parasitic capacitance coupling to other parts of the IC, such as the substrate. Though additional process steps may be needed for the resistors, it may be possible to alternatively use the diffusions steps, such as the N and P implants that make up the drains and sources of the MOS devices. The shortcomings of these elements as resistors, as can the poly silicon gate used as part of the CMOS devices. The shortcomings of these elements as resistors, beyond their high parasitic capacitances, are the resistor's high temperature and voltage coefficients and the limited control of the absolute value of the resistor.

Even with these additional process steps, analog engineers must cope with small capacitor sizes (50-pf maximum) and variations in the absolute value of both the resistors and capacitors (with no tracking between the resistors and capacitors that could stabilize the resistor-capacitor-capacitor time constraint (RC) product). Analog designers have developed novel circuits, such as switched capacitor circuits, to surmount these obstacles. Indeed, CMOS enable the switched-capacitor circuit.

Beyond component consideration, circuit layout must be done carefully to prevent digital switching noise from degrading circuit performance. For example, power supply routing must be carefully managed in analog circuits. The quality of computer models for active and passive components is also a thorny issue. Models that are sufficiently accurate to estimate the speed performance, of digital gates are not accurate enough to predict gain or high-frequency response. Drain conductance, for instance, is a key analog design parameter, though it does not

affect digital gate speed. Thus, heightened attention to the modeling of active, passive, and parasitic components is needed for the circuit to perform as expected on its first pass through the silicon manufacturer. The introduction of RF circuits to an SOC creates numerous problems. The circuits are sensitive to noise on the power supply and substrate, owing to the low-level signals at which they operated and the likelihood of correlated digital noise mixing with the nonlinear RF components giving rise undesired spurs in the RF circuit's outputs. Moreover, RF circuits require their own set of active and passive components. Foremost is the need for a high-speed, low-noise bipolar transistor. CMOS devices have yet to demonstrate that they can be used in high volume RF systems with challenging specification such as those found in cellular phones while concurrently offering competitive power consumption and die area. If the RF SOC is to be competitive with a multiple-chip or discrete-components system, the bipolar devices available in the process that are intended for use in an RF SOC application must be state-of-the-art.

Inductors play a critical role in RF circuits, especially in low-noise amplifiers, mixers, filters, power amplifiers, and oscillators. The inductor enables the tuned narrow-band inductance-capacitance (LC) circuit. These circuits not only filter undesired signal, but also allow for the design of circuits that can operate over a narrow band at much higher frequencies than would be possible for a broadband design without inductors. Oscillators, with the very low-phase noise required by high-performance RF systems, also need LC tank circuits. For this application, high (larger than ten) Q-factors are required. Here, inductors are used for impedance matching, bandwidth extension through peaking of the response,

degeneration (extension of the linear range of operation at the cost of absolute gain) without the noise penalty of resistors, and as current sources. A current source allows for more headroom for the active devices than an active current source or a resistor. This is pivotal for battery-powered devices or designs that incorporate bipolar or MOS field-effect transistors (MOSFETs) with low breakdown voltages. Inductors must be available in an IC process that is to be used to form an RF SOC, given their role in RF circuits.

RF circuits place additional requirements on the on-chip resistors and capacitors. Resistors must be very linear, have minimal temperature coefficients, have better control of absolute accuracy, and demonstrate very low parasitic coupling to the substrate. Capacitors need high Q in RF systems. Absolute values of the capacitors may need to be much larger than those in an analog circuit when the capacitors are used for impedance matching, bypassing, or phase-locked loop (PLL) filter applications.

Last, a voltage-controlled capacitor (varactor) is required to make RF voltage -controlled oscillators with low-phase noise. Varactors are paired with inductors to form the tuned circuit for the oscillator. A dc voltage coupled onto the varactor tunes the oscillator frequency. Varactors may be formed from reverse-biased junctions in a process. While the grading coefficient of the PN junction is not optimal for a large variation of capacitance with applied voltage, as in a discrete varactor, the junctions are still useable. PN junctions available in an IC process include the junctions of the PMOS (in the n-well process) and NMOS (in the p-well process) drains, as well as the bipolar BE or BC junctions. MOSFETs can also be used as varactors since their capacitance changes as the gate voltage

changes. Limitations of on-chip varactors include poor linearity across the tuning range, limited tuning range, and low Q. These limitations can affect circuit performance. In a PLL, for example, low varactor Q can cause high-varactor tuning voltage and the varactor capacitance can change PLL loop dynamics over the range of frequencies to which the PLL locks. A tight varactor tuning range and a large variation in the absolute capacitance value of the varactor will limit the PLL lock range.

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3. ACTIVE DEVICE OPTION FOR ANALOG AND RF

SOC DESIGN

3.1 BIPOLAR

Bipolar devices offer superior performance attributes for many analog and RF circuits. They can be more reliably modeled than CMOS devices at RF frequencies and exhibit less component variation than CMOS device at RF frequencies. The larger design margin between circuit requirements and device fundamental operating limits permits faster design cycle time and affords a higher success rate for first-time silicon. First-pass success is gaining importance, as the cost of a mask set used to process a deep sub-micron wafer can exceed US\$500,000. Early success is also desirable against the backdrop of increasing cycle times for wafer production, package preparation, and device testing.

Bipolar devices exhibit better device-to-device matching and, thus, allow lower input offset voltages. Bipolar devices are fundamental to voltage reference circuits, such as band gap reference. Bipolar amplifiers exhibit lower noise, increased bandwidth, easier matching to off chip RF passive components, and higher gain for a given layout size and power consumption level. For a given current level, a bipolar device always has greater transconductance than a MOS device. Emitter-coupled logic (ECL) and current-mode logic (CML) bipolar gates operating at very high frequencies will have less power consumption than CMOS-based logic. The balanced current-steering structure of these logic families and the

small switching-voltage swing moderated the on-chip radiated noise in bipolar ECL and CML.

3.2 CMOS

In many analog and mixed-signal circuit designs, CMOS devices may be required. CMOS devices produce excellent switches with very high off resistance and no voltage drop when on. CMOS amplifier input stages require no dc current flow for bias. The excellent performance of CMOS switches and the ability to build amplifiers with an infinite input resistance is fundamental to the development of switched-capacitor circuits. These circuits are used in precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), as well as comparators and filters. CMOS devices biased in the triode region can be used as voltage-controlled resistors.

3.3 BiCMOS

BiCMOS technologies possess better integration capability than bipolar-only technologies. It is not possible to develop very-high-density digital circuits in bipolar-only technologies, as these bipolar logic circuits consume static power. Also of importance to SOC systems is the vast set of large macro cells, including microprocessors, memory macros, and DSPs, that are available in most CMOS technologies, as well as the computer-aided design (CAD) infrastructure for multi-million gate systems, that exist in fine-line CMOS technologies. In many analog and mixed-signal circuit block designs, the combination of MOS and bipolar devices results in an optimal circuit design.

BiCMOS usually can be classified in two categories: bipolar-based BiCMOS technology (BiCMOS optimized for high-performance bipolar transistors) and CMOS-based Bi-CMOS technology (BiCMOS optimized for high-speed CMOS devices). The former is often used for specialized applications where system integration may not be large, though bipolar performance must be maximized to ensure proper system creation. CMOS-based BiCMOS technology is designed for high-speed signal processing ICs that may span in size from small to large chips containing a complete communications system. Bipolar-based BiCMOS technology must provide its own digital CMOS infrastructure while achieving adequate return-on-investment to make the manufacturing line profitable. In contrast, CMOS-based BiCMOS technology takes advantage of the ever-increasing wafer size and scaled-down lithography of the most modern CMOS production line. The quality control and throughput optimization that is fundamental to any modern high-output CMOS fabrication facility (fab) is applied to the manufacturing process steps involving the bipolar device. In addition, the entire CMOS infrastructure, including modeling, standard cell libraries, large-scale macro cells, and CAD tool flows developed to design CMOS application specified ICs (ASICs), can be applied to CMOS-based BiCMOS technology is better suited for implementing low power wired- and wireless- communication SOC integrated circuits and meeting time-to market requirements than a BiCMOS process that is optimized for npn performance without preserving the characteristics of the corresponding generation of CMOS process that is optimized for npn performance without preserving the characteristics of the corresponding generation of CMOS technology.

The bipolar device should not introduce more than 10-30% additional costs relative to the standard CMOS device; this is key for high-volume use of BiCMOS as a SOC enabler. In addition, the BiCOMOS process must be available as soon as possible after the fine line CMOS process becomes available. If the development time for the bipolar module lags the CMOS by too long, it is more likely that a multiple, the BiCMOS process must be available as soon as possible after the fine line CMOS process becomes available. If the development time for the bipolar module lags the CMOS by too long, it is more likely that a multiple-chip solution engineered from different device technologies may be preferred to a single SOC implementation. It is, however, a challenging task to integrate the RF bipolar module into a signal-processing core CMOS process without disturbing the CMOS device characteristics and/or delaying deployment of the process. Moreover, the bipolar process should not require a wealth of additional process equipment that increases the cost to the fab and affects cycle-time optimization for all process technology run in the fab.

4. BiCMOS PROCESS TECHNOLOGY FOR MIXED- RF, DIGITAL, AND ANALOG CIRCUITS

Along with active elements, modern RF and analog-circuit designs require high-quality passive components, including resistors, capacitors, inductors, and varactors. As with the bipolar device, it is essential that these components integrate into the core CMOS process with a minimum of cost adders or extension of the time to process introduction.

In this section, we look at a CMOS-based Bi-CMOS process technology that incorporates high-performance SiGe bipolar transistors, high-Q inductors, capacitors, Varactors, and precision resistors as modules to a core 0.14- μm CMOS process technology and is, thus, compatible with the requirements of mixed-signal SOC integrated circuits. While the information to follow is specific to the process developed at Agere Systems for production on 8-in wafers at the company's Orlando, Florida, fab, many of the techniques described are also finding their way into process technology from other manufactures.

4.1 Technology Description of the Standard Deep-Submicron CMOS Process

4.1.1 Digital CMOS Core Process

The core 0.14- μm CMOS process; upon which the bipolar and passive modules will be added, uses p-epi/p substrate, shallow oxide trench isolation (STI), dual-gate oxides to support high-and low-breakdown voltage devices and

dual-doped (P+ for PMOS devices and n+ for NMOS devices) tungsten polycide (WSI)- to reduce gate resistance-gates. The dual-doped gates ensure that both the PMOS and NMOS devices operate in the surface, not buried, channel mode of operation to reduce leakage. This allows for low NMOS and PMOS thresholds that facilitate operation below 1.5 V. The process also offers up to seven aluminum metal levels with tungsten plug vias (contacts) and inter-level dielectric with dielectric constants lower than traditional silicon dioxide. The high-performance 1.5-V NMOS and PMOS transistors feature 0.135- μm minimum gate length and 2.4-nm gate oxide, resulting in a ring oscillator delay of 22 ps/stage. Low-power NMOS/PMOS transistors are also available in the CMOS process with low off current of 10 pA/ μm . The vast majority of CMOS devices on the chip will use these devices to reduce power consumption when the gates are not active. Increasing the threshold voltages and slightly increasing channel length reduces leakage.

In addition, 3.3-V NMOS/PMOS transistor with aggressive 5.0-nm gate oxide and high-drive currents of 700/400- $\mu\text{A}/\mu\text{m}$ are needed in the analog and RF portions of the circuits where a 1.5-V supply is not adequate for dynamic range requirements. Low supply voltages limit the number of devices that can be stacked, complicating the design of mixers and other circuit types. The vast majority of the digital gates must operate with the lower 1.5 V to reduce digital noise injected into the substrate. Noise injected in the substrate is a major problem when designing a mixed-digital/analog and RF systems, since this noise can degrade circuit performance.

4.1.2 Dense SRAM

Modern digital systems are memory intensive, and cell size is directly correlated with memory size; therefore, small cell sizes are required to fabricate memories of reasonable size. For example, the standard six-transistor static random access memory (SRAM) cell for this technology has an area of $5.7 \mu\text{m}^2$. A dense modular SRAM cell with an area of $3.3 \mu\text{m}^2$ is also available by tightening selected design rule and with the addition of one mask level for a self-aligned and borderless contact. Nonvolatile memory cells are also used to implement redundancy in dense memory arrays; this adds another modular process sequence and uses one additional mask level. Buried fusible links are available when only a few bits are required, for example, when trimming voltage references or building in chip IDs

4.1.3 PROCESS INTEGRATION OF THE SiGe DEVICE

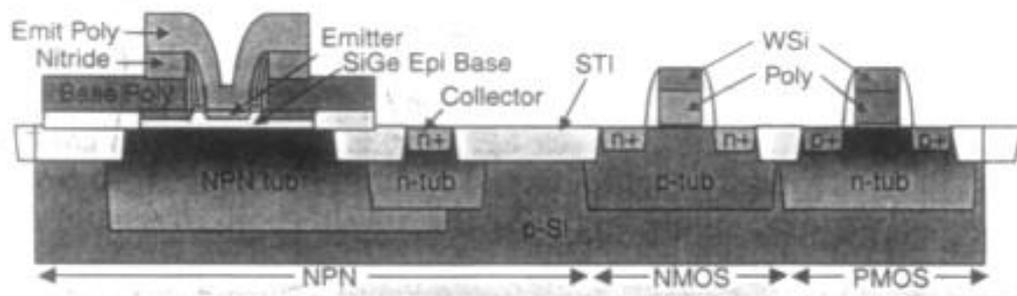


FIGURE1 SiGe BiCMOS Schematic cross section

Next consider the low-cost integration of SiGe bipolar devices with the core CMOS process for mixed RF, analog, and digital SOC chips. Figure 1 shows a cross section of the silicon wafer with both the CMOS and SiGe bipolar devices. The addition of a SiGe bipolar transistor module introduces a low-cost, high-performance, super-self-aligned (double-poly) graded SiGe base NPN transistor to the CMOS process. In a double polysilicon bipolar transistor, the base and emitter polysilicon define the placements of the base and emitter regions, respectively. The emitter is formed using arsenic-doped poly. The capacitances from emitter to base (C_{eb}) and from base to collector (C_{cb}) are reduced because no extra implant width is required to account for registration errors between the active element of the device and its contact.

The NPN transistor module requires just four additional mask levels, using high-energy phosphorous implantation for the sub-collector and selective epitaxy for the SiGe base. The SiGe bipolar module does not alter the 0.14- μm digital CMOS device parameters. Standard shallow trench isolation is used to isolate bipolar transistors.

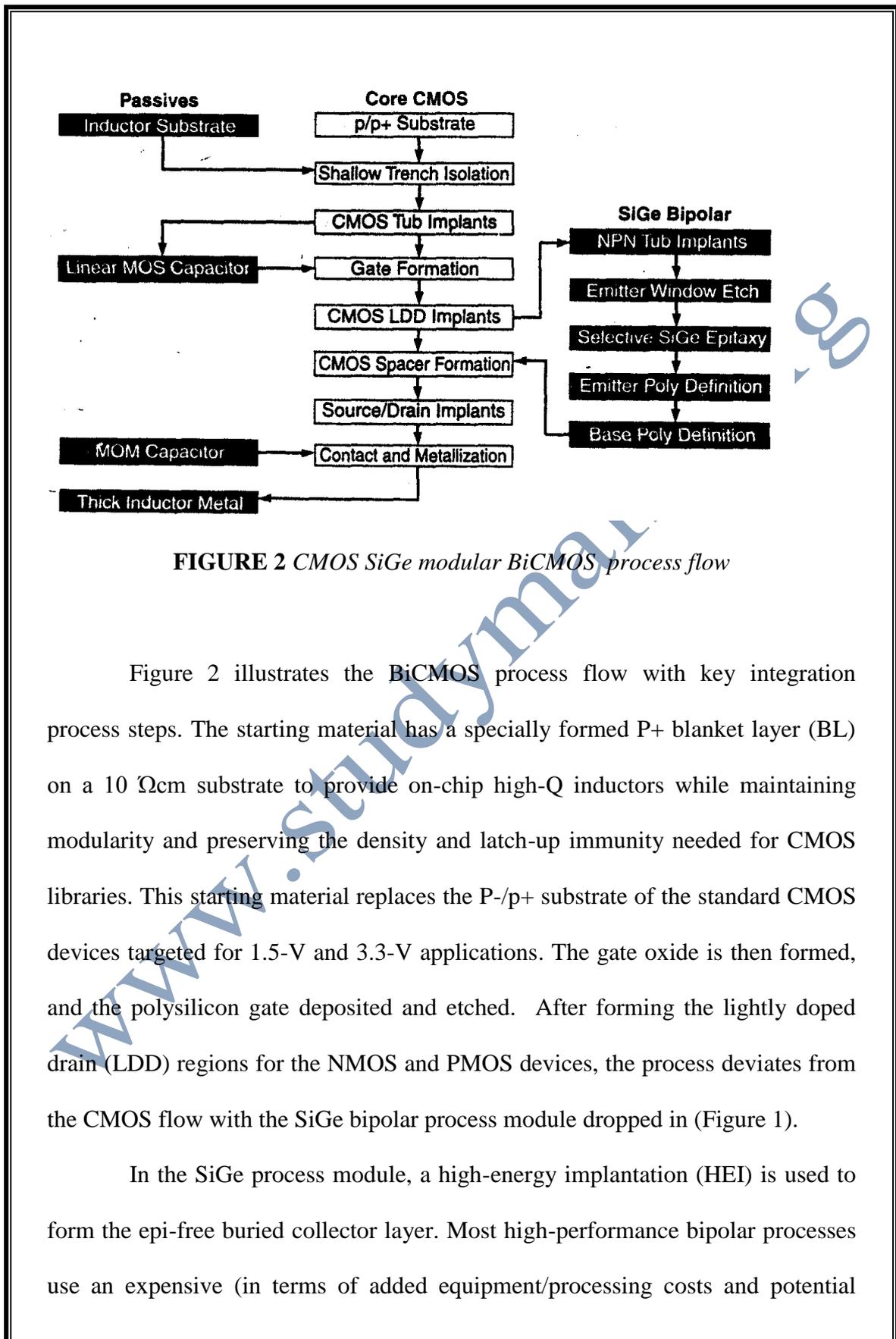


FIGURE 2 CMOS SiGe modular BiCMOS process flow

Figure 2 illustrates the BiCMOS process flow with key integration process steps. The starting material has a specially formed P+ blanket layer (BL) on a 10 Ωcm substrate to provide on-chip high-Q inductors while maintaining modularity and preserving the density and latch-up immunity needed for CMOS libraries. This starting material replaces the P-/p+ substrate of the standard CMOS devices targeted for 1.5-V and 3.3-V applications. The gate oxide is then formed, and the polysilicon gate deposited and etched. After forming the lightly doped drain (LDD) regions for the NMOS and PMOS devices, the process deviates from the CMOS flow with the SiGe bipolar process module dropped in (Figure 1).

In the SiGe process module, a high-energy implantation (HEI) is used to form the epi-free buried collector layer. Most high-performance bipolar processes use an expensive (in terms of added equipment/processing costs and potential

yield loss) epitaxial BL to reduce the extrinsic collector resistance. The BL also introduces significant deviation from the core CMOS process. An alternative is high-energy ion implantation to replace the BL. This implantation step challenges process technologists because it is a deep, high-dose implant. Control of implant and preventing silicon surface damage are keys to successful HEI.

A thick photo-resist layer covers the CMOS area on the wafer during HEI to prevent contamination by the implant. The photo-resist layer is specially treated by extended thermal baking and UV hardening before HEI to prevent resist cracking and peeling during HEI.

An insulating oxide layer is deposited after HEI, then, a layer of amorphous polysilicon is deposited. The polysilicon layer will form the extrinsic base contact for the bipolar device. The transistor's extrinsic base is heavily doped with p+ boron to reduce base resistance. A thick nitride layer on top of the amorphous silicon base provides isolation between the base polysilicon and the emitter polysilicon that will be deposited later. After cutting the emitter window through the nitride and amorphous silicon stack, an optional selective collector implant (SIC) is introduced (Figure 3)

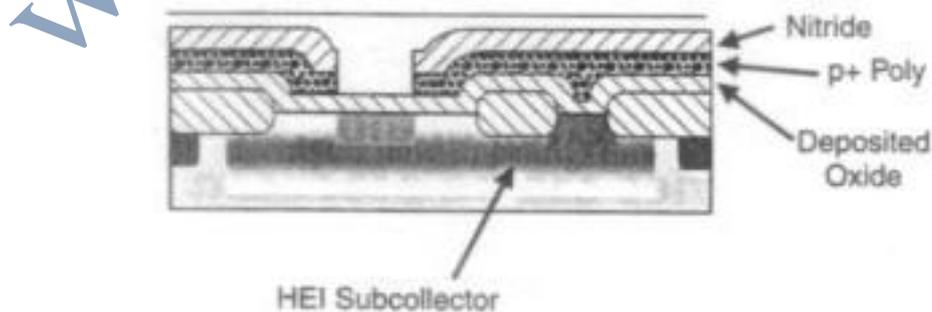


FIGURE 3 Cross section after cutting the emitter window

SIC implantation is normally performed only for transistors that are to have a low breakdown-voltage. High-breakdown voltage transistors do not require this implant. Thus, fabricating both high and low breakdown devices in the same circuit requires five mask levels beyond the normal CMOS flow, although products requiring only one breakdown voltage can be fabricated with four mask levels beyond the standard CMOS flow.

A thin nitride spacer is then formed in the emitter window on the sidewall to prevent growth on the exposed extrinsic base poly during the following SiGe base growth. A timed 100:1 hydrofluoric acid (HF) dip etches away the remaining insulation oxide in the emitter window and creates a lateral gap between the base poly and silicon substrate (Figure 4)

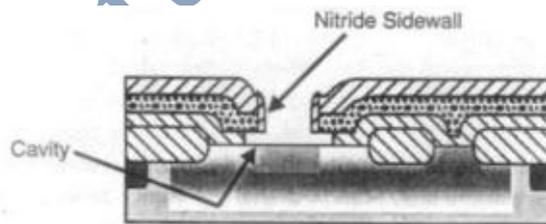


FIGURE 4 *Cross section after cavity created*

The SiGe base is selectively grown in the emitter window and fills the lateral gap to form good contact to the extrinsic base poly (Figure 5).

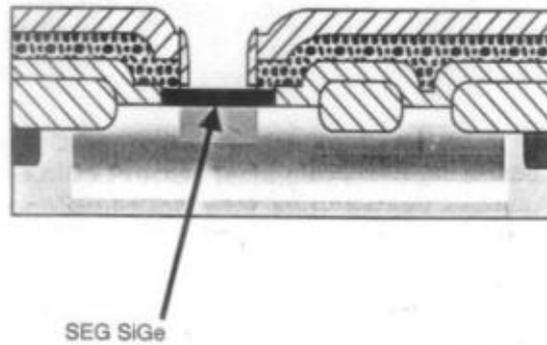


FIGURE 5 Cross section after SiGe growth

The base consists of a 30-nm undoped Si_{0.88}Ge_{0.12} layer together with a 30-nm boron-doped graded SiGe layer, where the Ge concentration is linearly ramped from about 12% down to 0%. Last, a 45-nm boron-doped Si layer is grown to cap the graded Ge region.. No growth on the nitride spacer is observable. The surface is very smooth and free of any particles and defects.

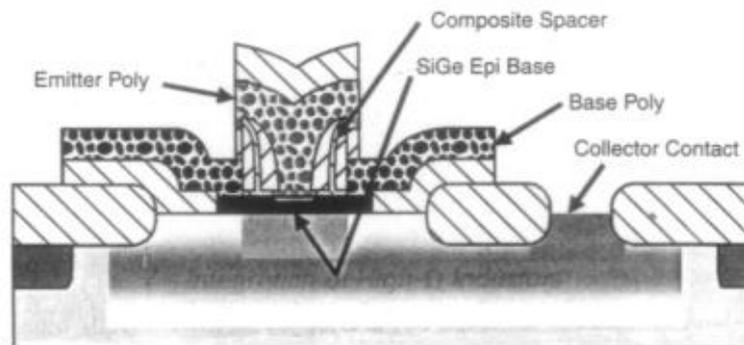


FIGURE 6 *Final SiGe device cross section*

The bipolar modules is completed by the lithography and etching of both the emitter and base polysilicon.

After the SiGe module, the BiCMOS process merges back to the CMOS flow to complete the source and drain (S/D) implant and anneal, as well as back-end process up to seven layer of metalization. At the conclusion of the process, the SiGe bipolar is shown in the scanning electron microscope (SEM) micrograph in Figure7

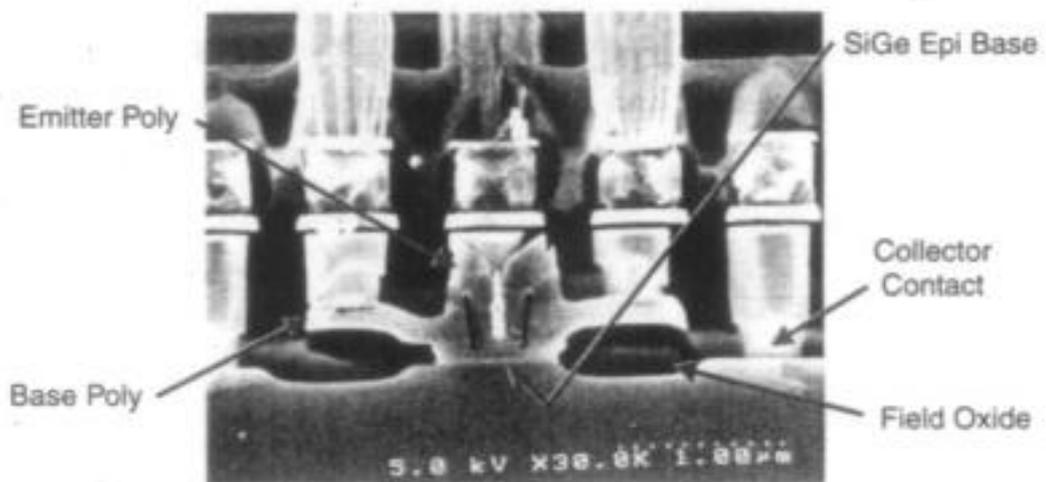


FIGURE 7 *SEM micrograph of device structure*

Table 1 summarizes the performance of the SiGe NPN transistors made in this process technology.

	High breakdown	High speed
Minimum emitter size	0.28 X 0.28 μm^2	0.28 X 0.28 μm^2
Emitter size for data in table	0.28 X 0.84 μm^2	0.28 X 0.84 μm^2
Beta	90	100
V_A	60	50
BV_{CEO}	3.6	2.5
BV_{CBO}	12.0	10.0
$f_t(\text{GHz})$ at $V_{CE}=3V/2V$	58	75
$f_t(\text{GHz})$ at $V_{CE}=3V$	37	50
$f_{max}(\text{GHz})$ at $V_{CE}=3V/2V$	102	104
f_{max} at $V_{CE}=3V$	54	52
$C_{BE}(\text{Ff})$	13.5	13.5
$C_{BC}(\text{Ff})$	9.0	12.4
$C_{CS}(\text{Ff})$	29.7	29.7
$N_{fmin}(\text{dB})$	0.5	.5

TABLE 1

The performance of both the high breakdown (collector-emitter breakdown of 3.6V) and high speed (collector-emitter breakdown of 2.5 V) bipolar devices are shown in Table 1.

The reduced breakdown voltage of the high-speed device is attributable to the changing implants that create a more heavily doped collector region, thereby increasing the multiplication factor at given reverse bias. As a trade-off, the device f_r increases from 58-78 GHz. As stated earlier, the process is designed so that multiple breakdown voltage devices are made available by the introduction of a mask that changes the collector implant doses. With multiple transistors, circuits that require large dynamic ranges or those that output significant power or interface to circuits outside the chip with 1.3-V swing will use the large breakdown voltage transistor. Those circuits requiring the highest speed performance, such as CML and low-level signal processing elements like receive-channel pre-amps and mixers, use the lower breakdown voltage device.

5. PASSIVE COMPONENTS FOR FULLY INTEGRATED ANALOG AND RF CIRCUITS

Several passive components are required to fully integrate analog and RF circuits in mixed-signal SOC ICs. These included analog resistors and capacitors, inductors, and varactors. This section describes how these elements can be realized in the aforementioned BiCMOS process.

In the process technology presented in this article, two high-density linear capacitors are available. Each requires one additional mask level to implement. The metal-oxide-metal (MOM) capacitor is designed for applications that require excellent linearity with a very low voltage coefficient (less than 40 ppm/V), and features a density of 1.0 fF/ μm^2 . The MOM capacitor is formed by deposition of a 35-nm oxide layer between the layers of a standard Ti/TiN/Al metal stack. The multiple metal layers of standard CMOS are required to reduce, metal migration under an applied field. This capacitor requires the process step of oxide deposition, a photolithographic step to define the capacitors, an oxide etch, and a photo strip. The processed adds no thermal cycles. The matching of a metal-metal capacitor to an adjacent capacitor depends on the accuracy of the etching of the capacitor. In a modern deep-submicron CMOS process, etching must be very well controlled since metal-to-metal spacing is 0.2 μm or less. Assuming careful layout, the MOM capacitor can match to better than 0.1% level as a result of this

careful etch control. This allows the development of data converters of 10 b or more without calibration or trimming.

Since the capacitor is made from metal, its series resistance is reduced. In turn, the capacitor's effective Q is raised. The capacitor can be placed high up in a multiple metal stack, allowing significant reduction of the parasitic capacitance to substrate when compared to poly-poly capacitor.

For applications that require higher density, such as bypass capacitors, a linear MOS capacitor is available with a voltage coefficient of 0.4%/V and density of 6.0 fF/ μm^2 . The linear MOS capacitor used the 5.0-nm gate oxide from the 3.3-V CMOS process with an additional arsenic implant to improve linearity.

5.1 RESISTORS

Several resistors are available in BiCMOS process technology and are summarized in Table 2.

	Sheet res.(Ω/sq)	Volt.Coeff.(ppm/V)	Temp Coeff(ppm/C)
N+ poly	16	-427	386
N+ diff	70	1167	1449
P+ diff	160	1502	1181
N-tub	670	7150	3312
NPN emitter poly	115	< 20	-974
NPN std base poly	80	< 20	1266

NPN	precision	300	< 20	635
base poly				

TABLE2 RESISTOR PARAMETERS

Gate poly, n+ and p+ source/drain, and n-tub resistors are characterized from the digital CMOS process. The center value of these resistors may vary as adjustments are made in the core CMOS transistor for optimal performance and yield. The diffusion resistors have high parasitic capacitance, significant temperature coefficients, and linearity limitations. The most heavily used of these resistors is the n-tub, which has the highest resistivity used in circuits. It is also extensively used in circuits designed to be functional in the digital CMOS process. The poly gate has a lower resistivity as a result of the silicide process technology used in its formation. This results in a less dense resistor with potential significant variation. This is, however, the only linear resistor available in a standard digital process, unless special poly-resistor is available that has been designed a part of the ESD structure.

Emitter and base-poly resistors are available from the SiGe bipolar module. As with the diffusion resistors discussed above, the doping level of the emitter, and sometimes base poly, needs to be changed to optimize transistor performance and yield. This affects the nominal sheet resistance of the resistors. The precision base-poly resistor uses one additional mask to allow the sheet resistance to be tailored to a predetermined specification without disturbing the NPN transistor parameters. P-type base-poly resistors with targeted sheet resistance of 300 Ω /sq have demonstrated excellent performance for RF analog

applications. The sheet resistance values varied within $\pm 3.9\%$ across the wafer and the temperature co-efficient of the resistor is 300 ppm with good voltage linearity.

5.2 CAPACITORS

Without any modules, a CMOS process offers only the gate-semiconductor capacitance for capacitor formation. Not only is this highly nonlinear as the device transition from accumulation to depletion, but it also results in a parasitic junction capacitance on silicon side of the device that makes the capacitor incompatible for many circuits. Traditional CMOS processes designed for analog-and mixed-signal applications have included an extra layer of polysilicon to form a poly-poly capacitor. This capacitor is much more linear and its parasitic capacitance from the lower poly layer to the substrate is significantly reduced. The introduction of the capacitor in the middle of the CMOS device processing cycle, however, is a drawback because the thermal process affects all the implants that precede it. More vertical topography that will affect the achievement of planarity in the latter stages of the process is also required as metal layers are added. From the perspective of the RF designer, the high series resistance of a poly-poly capacitor is a major disadvantage, given its low Q value.

In the BiCMOS process technology, two high-density linear capacitors are available. Each requires one additional mask level to implement. The metal-oxide-metal (MOM) capacitor is designed for applications that require excellent

linearity with a very low voltage coefficient (less than 40 ppm/V), and features a density of 1.0 fF/ μm^2 . The MOM capacitor is formed by deposition of a 35-nm oxide layer between the layers of a standard Ti/TiN/Al metal stack. The multiple metal layers of standard CMOS are required to reduce, metal migration under an applied field. This capacitor requires the process step of oxide deposition, a photolithographic step to define the capacitors, an oxide etch, and a photo strip. The processed adds no thermal cycles. The matching of a metal-metal capacitor to an adjacent capacitor depends on the accuracy of the etching of the capacitor. In a modern deep-submicron CMOS process, etching must be very well controlled since metal-to-metal spacing is 0.2 μm or less.

Since the capacitor is made from metal, its series resistance is reduced. In turn, the capacitor's effective Q is raised. The capacitor can be placed high up in a multiple metal stack, allowing significant reduction of the parasitic capacitance to substrate when compared to poly-poly capacitor.

5.3 INDUCTORS

Conflicting substrate requirements limit the integration of high-Q inductors with high-performance CMOS devices. Inductors fabricated using CMOS technologies based on epi/p+ substrates [Figure 8a) are severely degraded because of eddy-current losses in the substrate, and typically maximum quality-factor Q reported on epi/p+ substrates is only 3. The p+ layer has a resistivity of roughly 0.01 $\mu\text{-cm}$ and plays an important role in latch-up suppression and impurity gettering (attracting heavy metals away from the silicon surface) in CMOS devices.

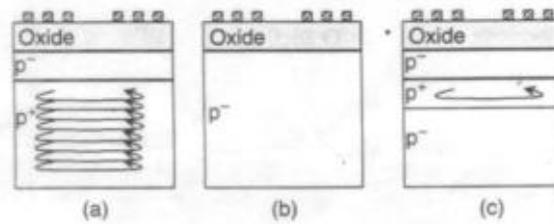


FIGURE 8

Substrate option for integrated inductors a) conventional epi/p+ substrate for latch up resistant CMOS technology has only low Q b) conventional P- bulk substrate for high Q inductors c) modified substrate for high Q inductors and latch up resistant CMOS.

The simple solution of changing to bulk substrate [Figure 8(b)] enables the fabrication of high- Q inductors but may exact a price in reduced device density (to prevent device latch up) and possible yield loss. Also, many of the reuse advantages in SOC integration would be voided. We next examine a modified substrate structure that addresses the conflicting goals of high Q and high from an established CMOS technology using epi/p+ substrates. Figure 8(c) shows the modified substrate structure that incorporates a blanket p+ BL positioned between a p- starting material and a p- epitaxial layer. The eddy current losses are limited to the thickness of the BL rather than the whole substrate, resulting in much higher inductor Q .

Silicon-on-insulator (SOI) is a recent advancement in process technology that can improve inductor Q . A 30% improvement in the quality factor of thick-aluminum inductors was measured, due to the absence of the p+ latch-up suppression layer.

5.4 VARACTORS

There are several options for implementing high-performance varactors. These can be categorized under two general headings: MOS and junction varactors. MOS varactors have been implemented using a non-inverting PMOS structure that can be realized by removing p+ source/drain implants from a PMOS transistor and replacing them with N implants. Several different types of junction varactors are feasible using some of the available options as viable possibilities. These are base-emitter, base-collector, and p-nub junctions.

Varactors have three important performance parameters: Q , C_{max}/C_{min} (maximum to minimum capacitance range over voltage), and tuning range (useful range over which the capacitance varies with voltage).

MOS varactors provide the best C_{max}/C_{min} (values as high as five have been achieved with the SiGe BiCMOS process). Base-emitter varactors have lower values (~ 2) while base-collector and p+-ntub varactors have similar but lower C_{max}/C_{min} (< 1.5). Highest quality factors over frequency can be achieved with MOS varactors, while base collector and p+-ntub varactors provide somewhat lower Q s. Base-emitter varactors have the lowest Q due to higher junction leakage. Although MOS varactors may provide the highest performance in terms of Q and C_{max}/C_{min} they suffer from lower tuning range.

6. BiCMOS TECHNOLOGY: PRESENT AND FUTURE

An application of the technology so far described is introduced by Agere systems, Orlando, Florida for a 10 GB/s 16:1 multiplexer and 10 GHz clock synthesizer. The chip integrates 4,000 bipolar and 3,100 MOS devices on a 5.5 X 5.5-mm die and is packaged in a 225-pin ceramic ball grid array. The 10-GHz oscillator core used MOM capacitors, pMOS varactors, base resistors, and a chip inductor with a Q of 16 at 10 GHz.

To extend this BiCMOS process in to next generation, Texas instruments is tapping the benefit of complementary SiGe bipolar transistor. TI has developed a third generation of fully isolated complimentary SiGe BiCMOS for ultra high speed precision analog and mixed signal IC s. this process is expected to go into volume manufacturing by the end of this year.

7. CONCLUSION

Presented an overview of a SiGe modular BiCMOS process technology. Through the use of add-on modules compatible with the core CMOS process technology, large-scale chips combining digital, analog, and RF technologies can be produced. Modules are added as required by the chip under development. By using the core process with added modules, the economies of scale associated with large-volume CMOS production are maintained without compromising the performance of the analog or RF circuits. By enabling higher-speed devices and increased device density levels, these exciting advances in process technology will decrease the number of ICs and discrete (passive) components required by complex optical, wired and wireless communication systems. As process technology advances, we will see SOC systems with millions of digital gates combined with RF circuits operating in the tens of GHz. This will be made possible through enhanced photolithographic scaling and, potentially, SOI technology that could result in faster devices and better isolation between circuit blocks. The ability to easily connect to the bodies of the MOS device remains a problem for SOI technology when the MOS devices are used in analog or RF circuits. Perhaps of greater significance will be the development of novel device structures and process technology innovations as catalysts for next-generation SOC systems.

8. REFERENCES

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