

A

Seminar report

On

Ovonic Unified Memory

Submitted in partial fulfillment of the requirement for the award of degree
Of MCA

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Preface

I have made this report file on the topic **Ovonic Unified Memory**; I have tried my best to elucidate all the relevant detail to the topic to be included in the report. While in the beginning I have tried to give a general view about this topic.

My efforts and wholehearted co-corporation of each and everyone has ended on a successful note. I express my sincere gratitude towho assisting me throughout the preparation of this topic. I thank him for providing me the reinforcement, confidence and most importantly the track for the topic whenever I needed it.

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Acknowledgement

I would like to thank respected Mr. and Mr.for giving me such a wonderful opportunity to expand my knowledge for my own branch and giving me guidelines to present a seminar report. It helped me a lot to realize of what we study for.

Secondly, I would like to thank my parents who patiently helped me as i went through my work and helped to modify and eliminate some of the irrelevant or un-necessary stuffs.

Thirdly, I would like to thank my friends who helped me to make my work more organized and well-stacked till the end.

Next, I would thank Microsoft for developing such a wonderful tool like MS Word. It helped my work a lot to remain error-free.

Last but clearly not the least, I would thank The Almighty for giving me strength to complete my report on time.

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Introduction

Ovonic unified memory (OUM) is an advanced memory technology that uses a chalcogenide alloy (GeSbTe). The alloy has two states: a high resistance amorphous state and a low resistance polycrystalline state. These states are used for the representation of reset and set states respectively. The performance and attributes of the memory make it an attractive alternative to flash memory and potentially competitive with the existing non volatile memory technology.

We are now living in a world driven by various electronic equipments. Semiconductors form the fundamental building blocks of the modern electronic world providing the brains and the memory of products all around us from washing machines to super computers. Semi conductors consist of array of transistors with each transistor being a simple switch between electrical 0 and 1. Now often bundled together in there 10⁶ of millions they form highly complex, intelligent, reliable semiconductor chips, which are small and cheap enough for proliferation into products all around us.

Identification of new materials has been, and still is, the primary means in the development of next generation semiconductors. For the past 30 years, relentless scaling of CMOS IC technology to smaller dimensions has enabled the continual introduction of complex microelectronics system functions. However, this trend is not likely to continue indefinitely beyond the semiconductor technology roadmap. As silicon technology approaches its material limit, and as we reach the end of the roadmap, an understanding of emerging research devices will be of foremost importance in the identification of new materials to address the corresponding technological requirements.

If scaling is to continue to and below the 65nm node, alternatives to CMOS designs will be needed to provide a path to device scaling beyond the end of the roadmap. However, these emerging research technologies will be faced with an uphill technology challenge. For digital applications, these challenges include exponentially increasing the leakage current (gate, channel, and source/drain junctions), short channel effects, etc. while for analogue or RF applications, among the challenges are sustained linearity, low noise figure, power added efficiency and transistor matching. One of the fundamental approaches to manage this challenge is using new materials to build the next generation transistors.

Review of memory basics

Every computer system contains a variety of devices to store the instructions and data required for its operation. These storage devices plus the algorithms needed to control or manage the stored information constitute the memory system of the computer. In general, it is desirable that processors should have immediate and interrupted access to memory, so the time required to transfer information between the processor and memory should be such that the processor can operate at, close to, its maximum speed. Unfortunately, memories that operate at speeds comparable to processors speed are very costly. It is not feasible to employ a single memory using just one type of technology. Instead the stored information is distributed in complex fashion over a variety of different memory units with very different physical characteristics.

The memory components of a computer can be subdivided into three main groups:

- 1) Internal processor memory: this usually comprises of a small set of high speed registers used as working registers for temporary storage of instructions and data.
- 2) Main memory: this is a relatively large fast memory used for program and data storage during computer operation. It is characterized by the fact that location in the main memory can be directly accessed by the CPU instruction set. The principal technologies used for main memory are semiconductor integrated circuits and ferrite cores.
- 3) Secondary memory: this is generally much larger in capacity but also much slower than main memory. It is used for storing system programs and large data files and the likes which are not continually required by the CPU; it also serves as an overflow memory when the capacity of the main memory is exceeded. Information in secondary storage is usually accessed directly via special programs that first transfer the required information to main memory. Representative technologies used for secondary memory are magnetic disks and tapes.

The major objective in designing any memory is to provide adequate storage capacity with an acceptable level of performance at a reasonable cost.

Memory device characteristics

The computer architect is faced with a bewildering variety of memory devices to use. However; all memories are based on a relatively small number of physical phenomena and employ relatively few organizational principles. The characteristics and the underlying physical principles of some specific representative technologies are also discussed.

Cost:

The cost of a memory unit is almost meaningfully measured by the purchase or lease price to the user of the complete unit. The price should include not only the cost of the information storage cells themselves but also the cost of the peripheral equipment or access circuitry essential to the operation of the memory.

Access time and access rate:

The performance of a memory device is primarily determined by the rate at which information can be read from or written into the memory. A convenient performance measure is the average time required to read a fixed amount of information from the memory. This is termed read access time. The write access time is defined similarly; it is typically but not always equal to the read access time. Access time depends on the physical characteristics of the storage medium, and also on the type of access mechanism used. It is usually calculated from the time a read request is received by the memory and to the time at which all the requested information has been made available at the memory output terminals. The access rate of the memory is defined as the inverse of the access time.

Clearly low cost and high access rate are desirable memory characteristics; unfortunately they appear to be largely incompatible. Memory units with high access rates are generally expensive, while low cost memory are relatively slow.

Access mode-random and serial:

An important property of a memory device is the order or sequence in which information can be accessed. If locations may be accessed in any order and the access time is independent of the location being accessed, the memory is termed as a random access memory.

Ferrite core memory and semiconductor memory are usually of this type. Memories where storage locations can be accessed only in a certain predetermined sequence are called serial access memories. Magnetic tape units and magnetic bubble memories employ serial access methods.

In a random access memory each storage location can be accessed independently of the other locations. There is, in effect, a separate access mechanism, or read-write, for every location. In serial memories, on the other hand, the access mechanism is shared among different locations. It must be assigned to different locations at different times. This is accomplished by moving the stored information, the read write head or both. Many serial access memories operate by continually moving the storage locations around a closed path or track. A particular location can be accessed only when it passes the fixed read write head; thus the time required to access a particular location depends on the relative location of the read/write head when the access request is received.

Since every location has its own addressing mechanism, random access memory tends to be more costly than the serial type. In serial type memory, however the time required to bring the desired location into correspondence with a read/write head increases the effective access time, so access tends to be slower than the random access. Thus the access mode employed contributes significantly to the inverse relation between cost and access time.

Some memory devices such as magnetic disks and drums contain large number of independently rotating tracks. If each track has its own read-write head, the track may be accessed randomly, although access within track is serial. In such cases the access mode is sometimes called semi random or direct access. It should be noted that the access is a function of the memory technology used.

Alterability-ROMS:

The method used to write information into a memory may be irreversible, in that once the information has been written, it cannot be altered while the memory is in use, i.e., online. Punching holes in cards and printing on paper are examples of essentially permanent storage techniques. Memories whose contents cannot be altered online are called read only memories. A Rom is therefore a non alterable storage device. ROMs are widely used for storing control programs such as micro programs. ROMs whose contents can be changed are called programmable read only memories (PROMs).

Memories in which reading or writing can be done with impunity online are sometimes called read-write memories (RWMs) to contrast them with ROMs. All memories used for temporary storage are RWMs.

Permanence of storage:

The physical processes involved in storage are sometimes inherently unstable, so that the stored information may be lost over a period of time unless appropriate action is taken. There are important memory characteristics that can destroy information:

1. Destructive read out
2. Dynamic volatility
3. Volatility

Ferrite core memories have the property that the method of reading the memory alters, i.e., destroys, the stored information; this phenomenon is called destructive read out (DRO). Memories in which reading does not affect the stored data are said to have nondestructive readout (NRDO). In DRO memories, each read operation must be followed by a write operation followed by a write operation that restores the original state of the memory. This restoration is usually carried out by automatically using a buffer register.

Certain memory devices have the property that a stored 1 tends to become a 0, or viceversa, due to some physical decay processes. Over a period of time, a stored charge tends to leak away, causing a loss of information unless the stored charge is restored. This process of restoring is called refreshing. Memories which require periodic refreshing are called dynamic memories, as opposed to static memories, which require no refreshing. Most memories that using magnetic storage techniques are static. Refreshing in dynamic memories can be carried out in the same way data is restored in a DRO memory. The contents of every location are transferred systematically to a buffer register and then returned, in suitably amplified form, to their original locations.

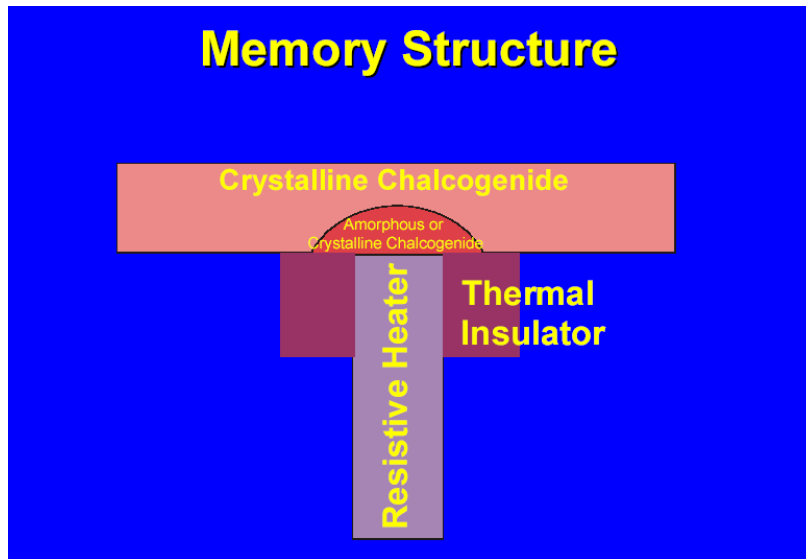
Another physical process that can destroy the contents of a memory is the failure of power supply. A memory is said to be volatile if the stored information can be destroyed by a power failure. Most semiconductor memories are volatile, while most magnetic memories are non volatile.

Cycle time and data transfer rate:

The access time of a memory is defined as the time between the receipt of a read request and the delivery of the requested information to its external output terminals. In DRO and dynamic memories, it may not be possible to initiate another memory access until a restore or refresh operation has been carried out. This means that the minimum time that must elapse between the initiations of two different accesses by the memory can be greater than the access time: this rather loosely defined time is called the cycle time of the memory.

It is generally convenient to assume the cycle time as the time needed to complete any read or write operation in the memory. Hence the maximum amount of information that can be transferred to or from the memory every second is the reciprocal of cycle time. This quantity is called the data transfer rate or band width.

Memory Structure



The above figure shows the memory structure of OUM

Key advantages of OUM

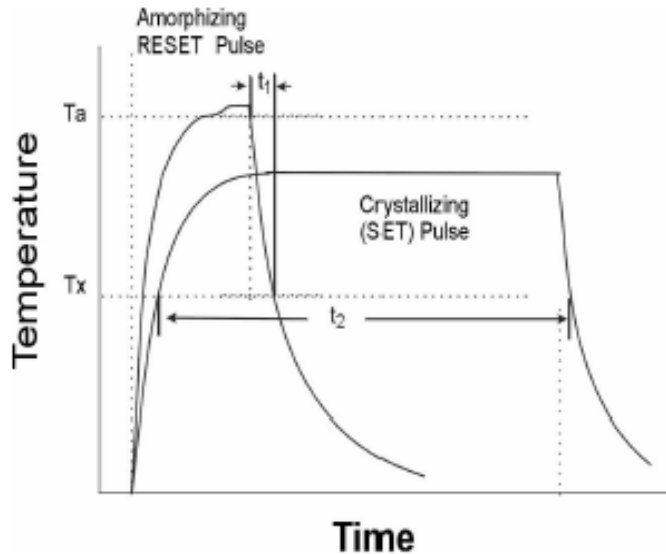
The following are the key advantages of OUM:

1. Endurance
2. Read-write performance
3. Low programming energy
4. Process simplicity
5. Cost
6. CMOS embeddability
7. Scalability

Write endurance is competitive with other potential non volatile memory technology, is superior to Flash. Read endurance is unlimited. The write/read performance is comparable to DRAM. The OUM technology offers overwrite capability, and bit/byte data can be written randomly with no block erase required. Scaling is a key advantage of OUM.

Write speed and write energy both scales with programmed volume. Its low voltage operation is compatible with continued CMOS feature and power supply scaling. Low voltage operation and short programming pulse widths yield low energy operation for the OUM, a key metric for mobile portable applications.

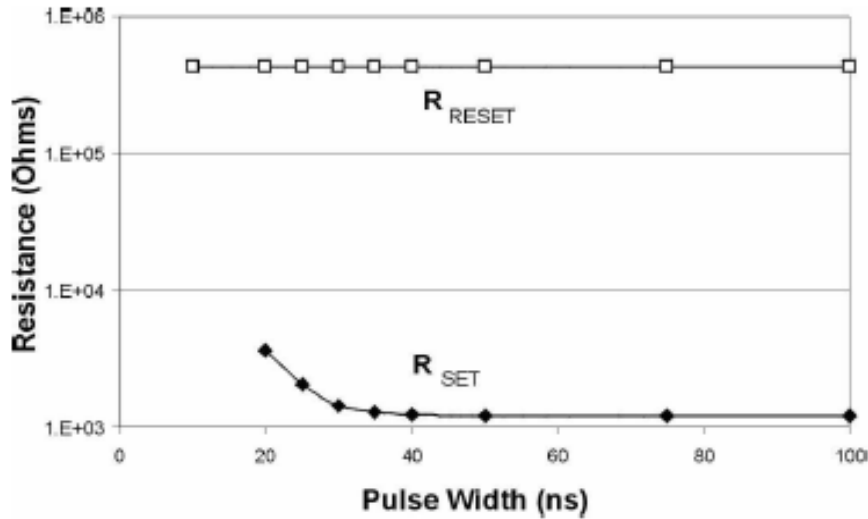
BASIC DEVICE OPERATION



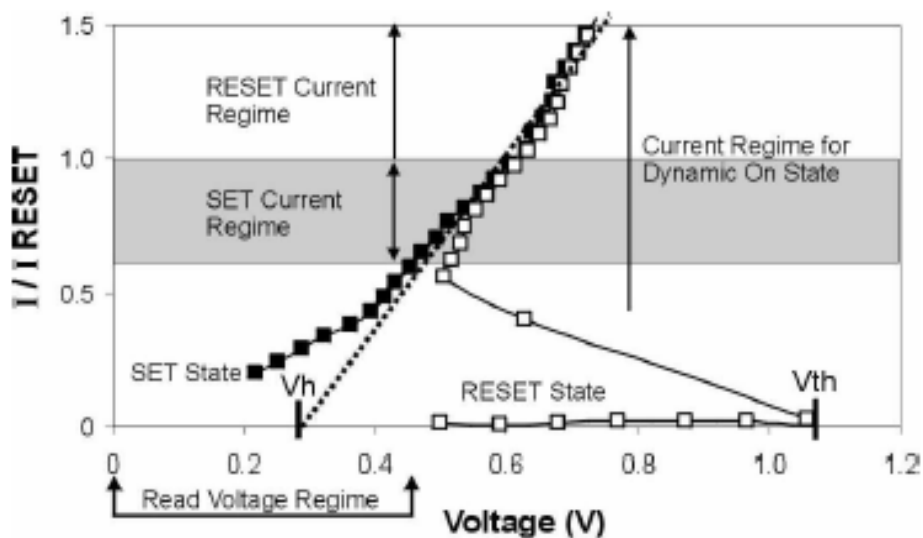
The basic device operation can be explained from the temperature versus time graph. During the amorphizing reset pulse, the temperature of the programmed volume of phase change material exceeds the melting point which eliminates the poly crystalline order in the material. When the reset pulse is terminated the device quenches to freeze in the disordered structural state. The quench time is determined by the thermal environment of the device and the fall time of the pulse. The crystallizing set pulse is of lower amplitude and of sufficient duration to maintain the device temperature in the rapid crystallization range for a time sufficient for crystal growth.

Technology and performance

The figure below shows device resistance versus write pulse width. The reset resistance saturates when the pulse width is long enough to achieve melting of the phase change material. The set pulse adequately crystallizes the bit in 50 ns with a RESET/SET resistance ratio of greater than 100.



I-v characteristics



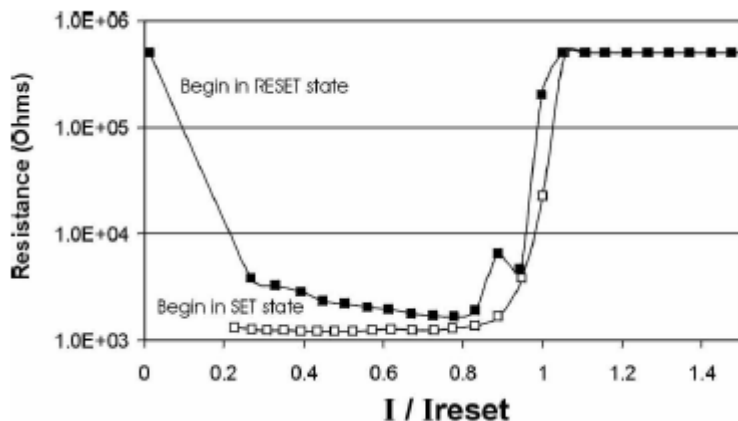
The figure above shows I-V characteristics of the OUM device. At low voltages, the device exhibits either a low resistance ($\sim 1k$) or high resistance ($>100k$), depending on its programmed state. This is the read region of operation. To program the device, a pulse of sufficient voltage is applied to drive the device into a high conduction “dynamic on state”. For a reset device, this requires a voltage greater than V_{th} .

V_{th} is the device design parameter and for current memory application is chosen to be in the range of 0.5 to 0.9 V. to avoid read disturb, the device read region as shown in the figure, is well below V_{th} and also below the reset regime.

The device is programmed while it is in the dynamic on state. The final programmed state of the device is determined by the current amplitude and the pulse duration in the dynamic on state.

The reciprocal slope of the I-V curve in the dynamic on state is the series device resistance.

R-I characteristics



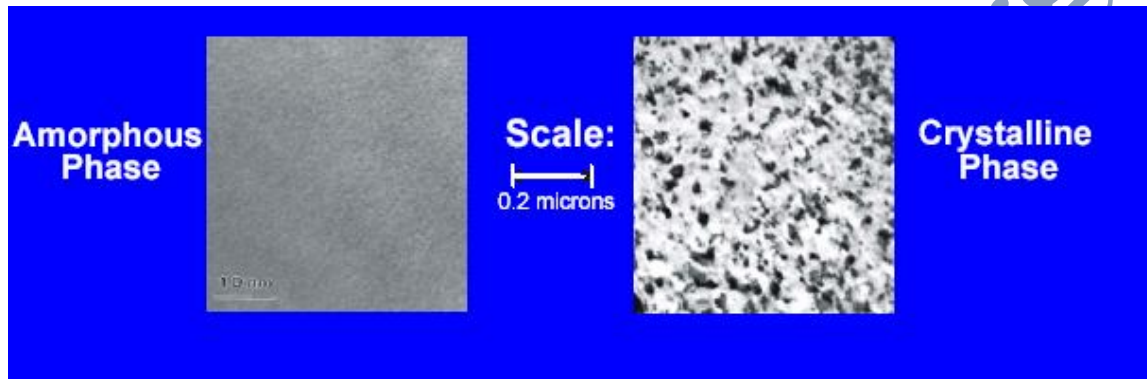
The above figure shows the device read resistance resulting from application of the programming current pulse amplitude. Starting in the set condition, moving from left to right, the device continues to remain in SET state as the amplitude is increased. Further increase in the pulse amplitude begins to reset the device with still further increase resetting the device to a standard amorphous resistance. Beginning again with a device initially in the RESET state, low amplitude pulses at voltages less than V_{th} do not set the device. Once V_{th} is surpassed, the device switches to the dynamic on state and programmed resistance is dramatically reduced as crystallization of the material is achieved. Further increase in programming current further crystallizes the material, which drops the resistance to a minimum value. As the programming pulse amplitude is increased further, resetting again is exhibited as in the case above. Devices can be safely reset above the saturation point for margin. Importantly, the right side of the curve exhibits direct overwrite capability, where a particular resistance value can be obtained from a programming pulse, irrespective of the prior state of the material. The slope of the right side of the curve is the device design parameter and can be adjusted to enable a multi- state memory cell.

Comparison of amorphous and crystalline states

Amorphous

Crystalline

Short range atomic order	Long range atomic order
Low free electron density	High free electron density
High activation energy	Low activation energy
High resistivity	Low resistivity



Conclusion

Non volatile OUM with fast read and write speeds, high endurance, low voltage/low energy operation, ease of integration and competitive cost structure is suitable for ultra high density ,stand alone and embedded memory applications. These attributes make OUM an attractive alternative to flash memory technology and potentially competitive with volatile memory technologies.

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